Electrical Properties of CSS Deposited CdTe Thin Films for Solar Cell Applications

N. K. Das
Dept. of EEE, Chittagong University of Engineering and Technology
Chittagong, Bangladesh,
nipudas@cuet.ac.bd

S. A. Razi
Dept. of EEE, Chittagong University of Engineering and Technology
Chittagong, Bangladesh,
razicuet@gmail.com

K. S. Rahman
Institute of Sustainable Energy
Universiti Tenaga Nasional
Kajang, Selangor, Malaysia
sajed_cuet_eee@yahoo.com

M. A. Matin
Dept. of EEE, Chittagong University of Engineering and Technology
Chittagong, Bangladesh
imamatin@yahoo.com

N. Amin
Institute of Sustainable Energy
Universiti Tenaga Nasional
Kajang, Selangor, Malaysia
nowshad@ukm.edu.my

***Abstract*— CdTe is a very potential absorber material for thin film solar cell application. In this work CdTe thin films (TF) were deposited on CdS thin films by close-spaced sublimation (CSS) technique at different source and substrate temperature in inert gas condition. To bring out the optimum temperature set for CSS deposited CdTe films, several experiments were done. The process pressure of the chamber during deposition was maintained at 1.5 Torr in a dynamic condition. The effects of deposition temperature on the electrical properties of the as-deposited CdTe films were investigated by Hall Effect measurement. The films were deposited at 610 ˚C, 630 ˚C, 650 ˚C and 670 ˚C source temperatures. The first three films showed p-type conductivity while n-type conductivity appeared in the film deposited at 670 ˚C. The hole concentration of the as-grown p-type CdTe films followed an upward trend with the increase of source temperature and it reached a peak value at 650 ˚C. The highest hole mobility was observed for the lowest source temperature. However, the resistivity of the CdTe films was found increasing with the increase of source temperature. Thus, the CdTe thin film deposited at 650 ˚C showed better electrical properties for solar cell applications.**

Keywords—CdTe thin film, Close-spaced sublimation, Electrical properties, Hall Effect measurement, Solar cells.

Introduction

CdTe is considered as a leading polycrystalline materials for the fabrication of highly efficient thin film (TF) hetero-junction solar photo-voltaic (PV) cells. Some unique physical properties make it an ideal p-type absorber material for solar PV cells. These properties include a direct band gap of about 1.45 eV which is optimum for the absorption of solar irradiation, an absorption coefficient which can be higher than 5×10^5 cm^{-1} at incident wavelengths of about 700 nm and the highest lattice parameter in the II-VI semiconductor group. Besides these, its formation energy is negative and the lowest among the members of this group. The CdS/CdTe based thin-film solar PV cells have already attained the efficiency over 22% in research level and over 18% in module level [1-2]. There are several techniques to deposit CdTe thin-films on CdS layer in which small-area laboratory solar cell demonstrate efficiency over 10% [3]. The most remarkable ones are CSS, electro-deposition, vacuum evaporation, sputtering, Vapor Transport Deposition (VTD), Metal Organic Chemical Vapor Deposition (MOCVD), Molecular Beam Epitaxy (MBE), and screen printing. All these techniques allow the deposition of high-quality thin films of CdTe which is polycrystalline in nature. However, the most efficient CdTe TF solar cells have been found with CdTe absorber layers deposited using CSS technique till to date [4]. Moreover, this technique is attractive among the researchers because of its high deposition rate, the simplicity of operation, and lower vacuum level during deposition and easiness of fabricating large volume commercial modules [5-6]. The most vital deposition parameters of CSS equipment are included; the temperature of source and substrate, the chamber pressure, the deposition time and the deposition atmosphere [7-11]. The photovoltaic conversion efficiency depends on the microstructure, optical and electrical properties of the as-grown CdTe thin film absorber layers which can be regulated by the deposition parameters. Researchers around the world are trying to find out the relationship between these properties and the deposition parameters [12]. The built-in bias voltage at equilibrium open circuit voltage V_{bi} is related to the carrier concentration of absorber and window material according to (1) [13].

$$V_{bi} = \frac{k\,T}{q} \ln\left(\frac{N_d N_a}{n_i^2}\right) \tag{1}$$

Where k is Boltzmann constant, N_a, N_d, and n_i are acceptor, donor and intrinsic carrier concentration per cm^3 of absorber and window layer, q is the charge of electron and T is the temperature. Larger built-in potential is desirable for separating light generated electron-hole pair in the absorber material. The short circuit current density Jsc is related to the parasitic series (R_s) and shunt resistance (R_{sh}) according to (2) [13].

$$J_{sc} = J_o\left[e^{\frac{(q(V-R_sJ_{sc})}{AkT}} - 1\right] - J_L + \frac{(V - R_sJ_{sc})}{R_{sh}} \tag{2}$$

Where A is the diode quality factor and J_o is the saturation current density. In this work, the CdTe thin films were deposited on 100 nm thick CdS thin films for four different source and substrate temperature. The temperature difference (ΔT) between source and substrate of the CSS equipment was kept at 30 ^{0}C. The source temperature was gradually increased from 610 ^{0}C to 670 ^{0}C in a steps of 20 ^{0}C. The dependence of several electrical properties such as carrier concentration, resistivity and carrier mobility of the as-deposited CdTe thin films were investigated by Hall Effect measuring system.

I. Experiment

The 3 cm × 3 cm borosilicate glass substrate was used to deposit CdTe TF by CSS techniques due to its better optical transmittance in the visible wavelength and higher strain point than soda lime glass [15]. The substrates were subject to cleaned by standard cleaning procedure. The substrates were scratched by the pen cutter in one side for marking and then scrubbed manually for 30 s each side with a nylon brush in soapy water. After that, the substrates were rinsed with warm deionized water and then cleaned ultrasonically by methanol, acetone, methanol and deionized water respectively at a temperature 50 ^{0}C for 15 minutes each. The clean substrates were dried with N_2 gas and then air anneal in a hot plate at 100 ^{0}C for 5 minutes. Finally, four cleaned substrates were mounted to the substrate holder in an RF sputtering machine. The distance between target and substrate was kept 7 cm. A 100 nm thick CdS film was deposited on each clean substrate by RF sputtering under 3.9 mTorr working pressure for 30 minutes using 99.99% pure CdS target of 2-inch diameter. During deposition Ar gas flow was maintained to 16 sccm through MFC controller. The RF power of the plasma gun was kept to 30 W while the substrate temperature was at 100 °C. The as-deposited CdS film shown in Fig. 1.

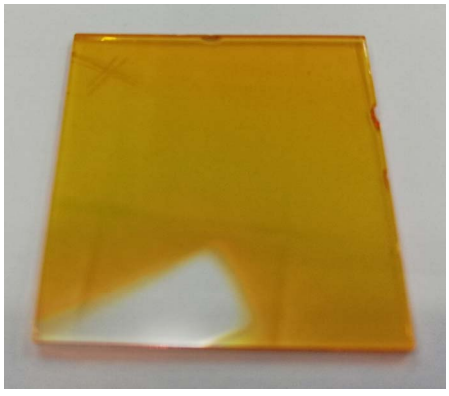

Fig. 1 RF sputtered as-deposited CdS films

The thickness of the CdS film was measured by the Quartz Crystal-deposition Monitor (QCM). The deposited CdS films were stored in a vacuum desiccator for avoiding the detrimental effects on the film-quality. The schematic diagram of traditional CSS equipment is shown in Fig. 2. The CSS equipment deposits CdTe film on one CdS film at a time. The 4N analytical grade CdTe powder was used as source material.

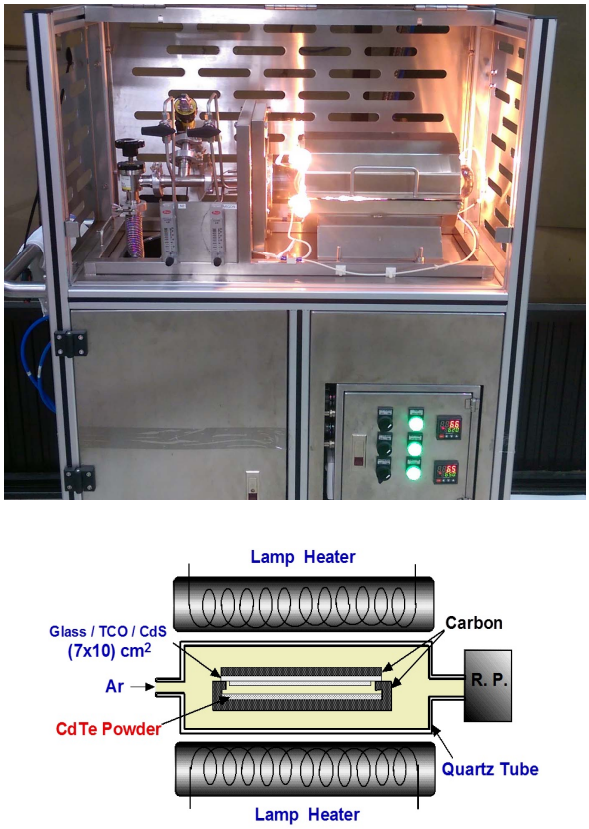

Fig. 2 CSS equipment with schematic diagram of chamber

The CdTe powder was poured into a graphite susceptor having 2.85 cm × 2.85 cm width, and 0.6 mm depth. The source powder was then compacted by a 2 cm× 5 cm glass slider. Finally, the CdTe powder was sintered to form a hard CdTe compound at 700 ^{0}C temperature for 30 minutes in Ar ambient. After that, the CdS film faced down towards the CdTe source as shown in Fig. 3.

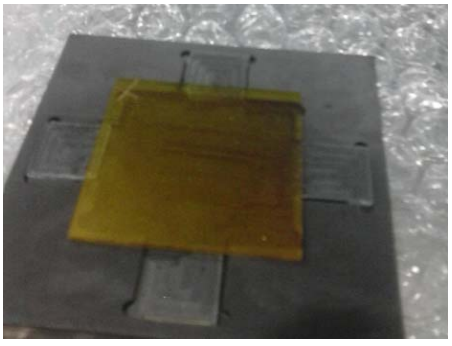

Fig. 3. CdS Films facing towards the CdTe Solid.

The important process parameters for depositing high-quality CdTe TF include the temperature of the source (T_{sou}) and substrate (T_{sub}), the spacing between source and

substrate, process pressure and process gas (Ar, He, or Mix) [3, 5]. The spacing between source and substrate was fixed at 2 mm and the process temperature was monitored by inserting thermocouple into the graphite susceptor and controlled by a PID controller. Two 2 kW tungsten halogen lamps were used, one at the bottom and the other at the top of the quartz tube for heating the source and substrate as illustrated in Fig. 2. The chamber was kept at a vacuum of 10 mTorr by a rough pump before deposition and then purged with highly pure N_2 gas. After that Ar gas was applied to the chamber. During the deposition, the chamber pressure was monitored by Instrutech pressure gauge and maintained at 1.5 Torr by regulating a throttle valve connected between the rough pump and the chamber. The CdTe films were deposited at four different source temperatures starting at 610 °C and then increased to 670 ^{0}C in three steps of 20°C equal increment while keeping the difference between the source and substrate temperature constant at 30 °C. The deposition time of each films were maintained to10 minutes. The as-deposited CdTe TF is shown in Fig. 4.

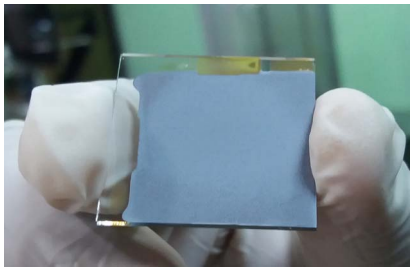

Fig. 4 As-deposited CdTe films on CdS films

II. Results and Discussion

The three major electrical properties including carrier concentration, mobility and resistivity of the as-deposited CdTe thin films were observed at room temperature by Hall/resistivity measurements. The ECOPIA Hall effect measurement system (HMS-3000) which is integrated with a resistivity measurement tool was used for this purpose. The system uses the van der Pauw method which is a four-probe method for the Hall measurements. During the measurements, a constant magnetic field was produced by using a pair of permanent magnets and then applied orthogonally to the upper surface of the films. Meanwhile, a DC (direct current) was made to pass through the thin film samples by using one of the two diagonal pairs of gold electrodes, electrically connected to a constant dc current source. The induced hall voltage was detected by the remaining electrode pair. The magnitude of the applied magnetic field was constant at 0.51 T. The type (p or n) of the CdTe films was denoted by the system using a positive (+) or negative (-) sign preceding the numerical value of the carrier concentration. The details results are discussed in the following subsections.

A. Effect of Temperature on Carrier Concentration

The calculation of the carrier concentration and mobility was done by the system itself using the magnitude of the induced hall voltage. Fig. 5 shows the effects of source temperature on the majority carrier concentration in the CdTe films. It is evident from Fig. 5 that the carrier concentration increases with the increase in source temperature. The values of carrier concentration were found 6.38×10^{11} cm^{-3}, 4.2×10^{12} cm^{-3}, 7.7×10^{12} cm^{-3}, and -6.78×10^{12} cm^{-3} for the samples deposited at source temperatures of 610 ^{0}C, 630 ^{0}C, 650 ^{0}C and 670 ^{0}C respectively. The highest carrier concentration was found in the sample deposited at 650 ^{0}C source temperature. As the photovoltaic conversion efficiency is directly related to the carrier concentration, the CdTe films deposited at this source temperature are expected to yield the more efficient solar cells than the films deposited at other source temperature which is very consistent with the results reported by the other researchers [4-6].

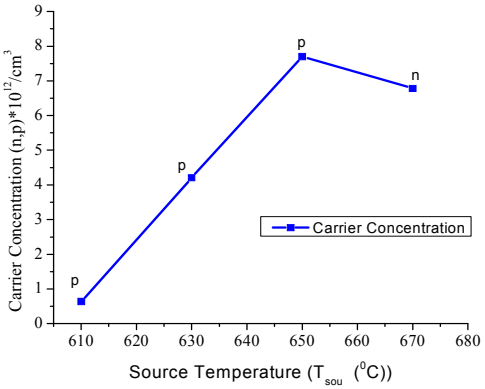

Fig. 5 Effect of temperature on CdTe TF carrier concentration

Another interesting observation is that, the CdTe films deposited at source temperatures higher than 650 ^{0}C become n-type semiconductor which is not expected in case of CdTe thin film solar cells because the CdTe is usually used as the p-type absorber layer. These might be happened for source temperature higher than 650 ^{0}C, where the sublimation rate of the cadmium atoms on the CdS layer surpasses that of tellurium atom. As a result, the percentage of cadmium becomes higher than the tellurium in the CdTe films and thus the films become n-type.

B. Effect of Temperature on Carrier Mobility

The variation of majority carrier mobility with the source temperature is shown in Fig. 6.

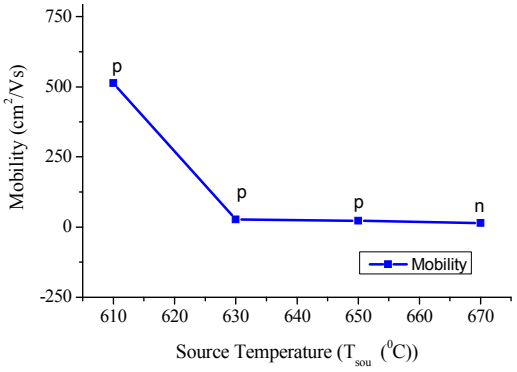

Fig. 6 Effect of temperature on CdTe TF carrier mobility.

In the figure it is observed that, hole mobility is highest (512 cm^2/Vs) in the sample deposited at 610 ^{0}C source temperature. As the source temperature increases from 610 ^{0}C to 630 ^{0}C, the hole mobility decreases significantly from

512 cm^2/Vs to 25 cm^2/Vs. After that, the rate of decrease in mobility become not significant. For the source temperature of 630 ^{0}C and 670 ^{0}C, the mobility was found to be 22 cm^2/Vs (hole) and 15 cm^2/Vs (electron) respectively. The decrease in carrier mobility with the increase in source temperature is agreeable with the theory. As the source temperature increases, the carrier concentration also increases. As a result the mean free path of the carriers decreases and the total number of collisions per carrier to travel a certain distance increases consequently decreasing the carrier mobility.

C. Effect of Temperature on Resistivity

The Fig. 7 demonstrates the change in film resistivity with the increase in source temperature is shown. It is clear from Fig. 7 that the resistivity shown an increasing trend with the increase in source temperature.

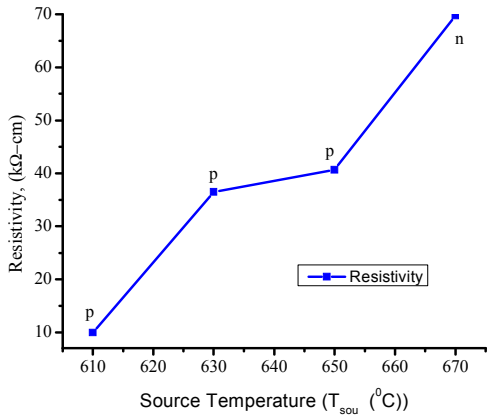

Fig. 7 Effect of temperature on CdTe TF resistivity

The resistivity was found 9.96 kΩ-cm, 38.6 kΩ-cm, 40.7 kΩ-cm and 70 kΩ-cm for the samples deposited at source temperature of 610 ^{0}C, 630 ^{0}C, 650 ^{0}C and 670 ^{0}C respectively. Among the p-type CdTe films, the highest resistivity was found in the sample for 650 ^{0}C source temperature. The resistivity of as-deposited CdTe films were lower than the results reported by the other researcher [15-18]. The n-type CdTe thin film offers the highest resistivity among the four CdTe TF samples. This may be because of the lowest mobility found in n-type CdTe as-deposited films.

In general, a higher carrier concentration, lower resistivity and higher mobility are desirable for the absorber layer to increase open-circuit voltage V_{oc}, fill factor FF and short-circuit current density J_{sc} of the solar cell. It is very difficult to achieve all these suitable properties in a single film. Therefore, in practice rigorous optimization is recommended for this purpose. Considering all the electrical properties finally it is concluded that, the CdTe film deposited at 650 °C source temperature is suitable as the absorber layer in solar cell applications.

III. CONCLUSION

The performance parameters of CdTe solar cell are directly depends on the micro-structural, electrical and optical properties of different functional layers. In CSS technique the direct phase transition occurs between the CdTe solid to gas state congruently. The main focus of the work was to investigate the temperature dependence of electrical properties of as grown CdTe TF. Both the p-type and n-type conductivity of CdTe TF were found for different source and substrate temperatures. The carrier mobility of the CdTe TF dramatically decreases for the source temperature increasing from 610 °C to 630 °C, whereas the resistivity of the CdTe TF increase with source temperature. The effects of the source and substrate temperature on the electrical properties of CdTe films were found consistent with the other related published works. The electrical properties of the CdTe TF at 650 °C source temperature were found to be better than the counterparts deposited in dynamic condition.

REFERENCES

[1] First Solar, "First Solar Series 6." [Online]. Available:http://www.firstsolar.com/Modules/Series-6. [Accessed: 19-Feb-2019].

[2] M. A. Green et al., "Solar cell efficiency tables (Version 53)," *Prog. Photovoltaics Res. Appl.*, vol. 27, no. 1, pp. 3–12, 2019.

[3] C.S. Ferekides, U. Balasubramanian, R. Mamazza, V. Viswanathan, H. Zhao, D.L. Morel, "CdTe thin film solar cells: device and technology issues," *Solar Energy*, vol. 77, pp. 823–830, 2004.

[4] J. Sites, A. Munshi, J. Kephart, D. Swanson, and W. S. Sampath, "Progress and challenges with CdTe cell efficiency," *2017 IEEE 44th Photovolt. Spec. Conf. PVSC 2017*, no. June, pp. 1–4, 2018.

[5] J. Britt and C. Ferekides, "Thin-film CdS/CdTe solar cell with 15.8% efficiency," *Appl. Phys. Lett.*, vol. 62, no. 22, pp. 2851–2852, 1993.

[6] X. Wu, "High-efficiency polycrystalline CdTe thin-film solar cells," *Sol. Energy*, vol. 77, no. 6, pp. 803–814, 2004.

[7] A. Seth, G.B. Lush, J.C. McClure, V.P. Singh, D. Flood, "Growth and characterization of CdTe by closespaced sublimation on metal substrates," *Solar Energy Materials & Solar Cells*, vol. 59, pp. 35-49, 1999

[8] A. Bosio, G. Rosa, and N. Romeo, "Past, present and future of the thin film CdTe/CdS solar cells," *Sol. Energy*, vol. 175 no. Nov 2018, pp. 31–43, 2018.

[9] Benjamin R Wakeling, " Close space sublimation of CdTe for solar cells and the effect of underlying layers," PhD Thesis, Dept. of Applied Science, Security and Resilience, Cranfield University, August 2009

[10] B.A. Korevaar , A. Halverson, J. Cao, J. Choi, C. Collazo-Davila, W. Huber, "High efficiency CdTe cells using manufacturable window layers and CdTe thickness," *Thin Solid Films*, vol. 535, pp. 229-232, 2013.

[11] Naba R. Paudel, Yanfa Yan, "Fabrication and characterization of high-efficiency CdTe-based thin-film solar cells on commercial SnO2:F-coated soda-lime glass substrates," *Thin Solid Films,* vol. 549, pp. 30–35, 2013.

[12] Russell M. Geisthardt, Marko Topic, James R. Sites, "Status and Potential of CdTe Solar-Cell Efficiency, *IEEE Journal of Photovoltaics*, vol. 5, no. 4, July 2015.\

[13] J. Nelson, *The physics of Solar Cells*, 1st ed. World Scientific Publishing Company, 2003.

[14] Samuel H. Demtsu, "Impact of Back-Contact Materials on Performance and Stability of CdS/CdTe Solar Cells," PhD thesis, Dept. of Physics, Colorado State University Fort Collins, Colorado, June, 2006.

[15] Bülent M. Başol, Brian McCandless, "Brief review of cadmium telluridebased photovoltaic technologies*," Journal of photonics for Energy*, vol. 4, pp. (040996) 1-11, Jun. 27, 2014.

[16] M.A. Flores Mendoz, R. CastanedoPe´rez, G. Torres Delgado, J. Ma´rquezMarı´n, A. Cruz Orea, O. Zelaya Angel, "Structural, morphological, optical and electrical properties of CdTe films deposited by CSS under an argon–oxygen mixture and vacuum," *Solar Energy Materials & Solar Cells*, vol. 95, pp. 2023–2027, 2011.

[17] F. M. T. Enam, K.S. Rahman, M. I. Kamaruzzaman, K. Sobayel, M. Aktharuzzaman, N. Amin, "An Investigation on Structural and Electrical Properties of Close-Spaced Sublimation Grown CdTe Thin Films in Different Growth Conditions," *Chalcogenide Letters*, vol. 14, no. 4, pp. 125 – 131, April 2017.

[18] Peng Gu, Xinghua Zhu, Jitao Li, Haihua Wu, Dingyu Yang, " Influence of sputtering power on structural, optical and electrical properties of CdTe thin films prepared by DC magnetron sputtering," *Journal of Materials Science: Materials in Electronics*, vol. 29, pp. 14635–14642, 2018.