Evaluation of Butterworth Coupling Arrangement and Line Trap Circuit for PLC Integrated Power System

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Abstract- **Coupling Circuits (CCs) and Line Traps (LTs) are the two most important elements of PLC-integrated power system networks. CCs are used for selectively injecting PLC signals into the network, whereas the LT is used to restrict the PLC signal from entering into areas of the network where such signals may damage equipment. In this paper, a Butterworth filter based CC and a T-type LT circuit have been modelled, simulated and evaluated. The objective was to design power systems complaint coupling and line trap circuits to operate within the CENELEC frequency band. The key finding is that sufficient performance can be achieved in terms of the insertion loss profile of the CC and LT when such circuits are designed using commercially available off-the-shelf components. For the designed CC, the insertion loss was measured as -3 dB in the 55 kHz to 100 kHz range. For the LT circuit, the insertion loss was measured as more than -53 dB. This ensures low attenuation of the PLC signal by the CC, and high attenuation by the LT.**

Index Terms**—Powerline communication, Coupling, Line-trap, CENELEC, Evaluation, Commercial.**

I. INTRODUCTION

Application of Powerline Carrier (PLC) systems in power system networks can be used in numerous smart grid applications such as controlling home appliances, monitoring of distributed generators, data communications, and fault detection in power system networks [1]. A complete PLC integrated power system network will be associated with lots of peripherals including CCs, LT units, line tuner, and impedance matching units. Amongst the above listed peripherals, the CCs and LTs are the most important elements in the design and operation of an efficient PLC integrated power system network. These two elements are often said to form the heart of a PLC system.

Most research in this area is focusing on the application of PLC systems, rather than how PLC transmitters can be efficiently coupled to networks with minimal signal losses. For example, works in [2, 3] have outlined the suitability of PLC techniques in smart metering applications. Milidius et al. [4-6] has worked on the implementation of a three-phase power line fault detection system using the PLC technique. There are also works, which investigated the possibility of establishing a data connection over the Single Wire Earth Return (SWER) network using the PLC technique [7-12]. Beyond this, few researchers have also worked on modelling and evaluation of LTs and coupling circuits [13-17]. However, there is not much research reported in the literature, which has focused on the evaluation of the coupling arrangement and LT unit on the same network and in the same frequency range. Existing works [13, 17] focus on individual analysis of these two vital components, rather than a holistic analysis including both. This paper aims to address this knowledge gap by considering both in the same network.

The CENELEC band of frequencies (9 kHz to 150 kHz) has been allocated for the use of power utilities. In a PLC-integrated power system, the CC and LT serves opposite purposes. CC is expected to permit the transmission of signals into the network in a given frequency range. The LT, on the other hand, must block signals in this same frequency range to prevent signals from entering into and interfering with the parts of the network such as substations and generation units.

The highlight in this paper is a wide-band study where the CC and the LT unit have both been analyzed for the same frequency band and in the same network. Others [10, 11] have individually analyzed these components, which is a weakness and knowledge gap as these must work together in harmony in real networks. Considering the aforesaid issues, in this paper, a Butterworth bandpass filter based CC and a wideband LT circuit have been modelled and evaluated.

The key objective, in this paper, is to discuss the modeling of Butterworth CCs and LT units and evaluate these in terms of insertion losses within the 45 kHz to 130 kHz frequency band. In terms of insertion loss, it was found that the Butterworth CC produces very low insertion loss (around -3 dB) in the designated frequency band, but the LT unit produces very high insertion loss (more than -53 dB) in the same band.

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The key feature of this work that separates it from other published work [18, 19] is the fact that commercially available capacitors have been used in modelling the designed CC and LT rather than building models based on non-commercially available values obtained from theoretical calculations. The significance of this work lies in the fact that the designed CC and LT will be appropriate for use within real power networks because they produce desirable results within the designated frequency band. The designated frequency band (55 kHz to 100 kHz) forms a portion of the CENELEC frequency band.

The organization of the paper is as follows: Section 2 summarizes the basic concept of the work with a schematic arrangement and Section 3 presents the modelling and simulation of the Butterworth filter. The modelling and evaluation of the LT circuit has been presented in Section 4, followed by discussion of results in Section 5 and conclusions in Section 6.

II. BASIC CONCEPT OF THE WORK

A schematic arrangement of the PLC-integrated power system network is shown in Fig. 1, which includes the PLC transmitters and receivers, coupling circuits, line traps, and the electrical network. The PLC modem can generate signals in the 1-500 kHz frequency range. The desired Butterworth CC is expected to attenuate all signals outside the 45 kHz to 130 kHz range, and only allow PLC signals within the designated frequency band to be transmitted onto the electrical network. The function of the LT, connected to either end of the network, is to block signals in the same frequency range from penetrating into substations.

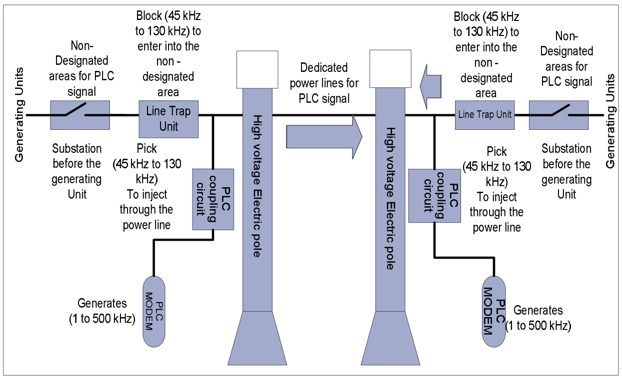

Fig.1 A PLC-integrated power system

III. MODELLING OF THE BUTTERWORTH COUPLING CIRCUIT

This section presents the modelling of the Butterworth filter type CC. The function of CC is to block the 50/60 Hz power frequency from entering into the PLC modem, but allow the high frequency PLC signals into the power line. Different types of filter circuits may serve this purpose such as the high-pass filters, the notch filter, and the band-pass filter.

As part of this research, the Butterworth type band-pass filter has been selected and modelled. There are two types of Butterworth filters, known as the π-type and T-type circuit arrangements. The Butterworth filter consists of different combination of LC pairs. Fig. 2 shows the π-type circuit arrangement and Fig. 3 shows the T-type circuit arrangement.

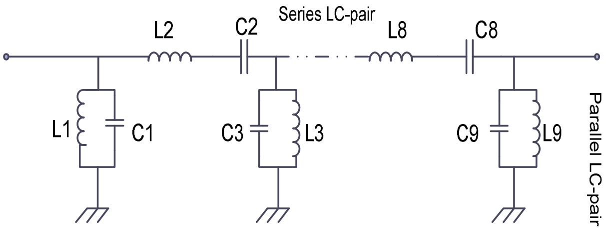

Fig.2 π-type Butterworth coupling circuit

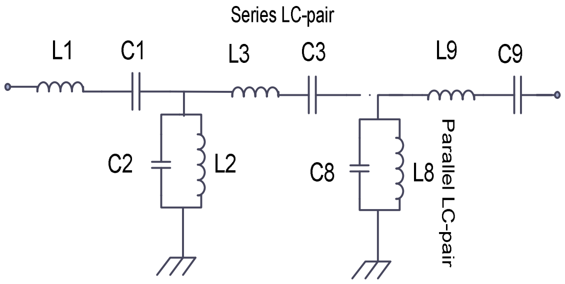

Fig 3 T-type Butterworth filter

The order of a filter, given by the number of cascaded pairs, has to be selected according to design requirements and the application area. The higher is the order of a filter, the sharper the slope of the filter would be. This is useful in applications such as military radio communication where a strict frequency band may be required.

To demonstrate the frequency response of a Butterworth filter, it is important to first calculate the value of the LC-pairs. The standard equations [18] that are used for calculating the filter LC-parameters are given in Eq. (1) to Eq. (4). Eq. (1) and Eq. (2) are used for calculating the inductance of the shunt and series connected inductors of the ith order respectively. Eq. (3) and Eq. (4) give the capacitances of the series and shunt connected capacitors of the ith order respectively.

$$L_{shunt} = \frac{g_i Z_0}{(2\pi)^2 BW \quad f_c} \tag{1}$$

$$L_{series} = \frac{BW \; * f_c Z_0}{g_i (2\pi \; f_c)^2} \tag{2}$$

$$C_{series} = \frac{g_i}{(2\pi) BW \quad Z_o} \tag{3}$$

$$C_{shunt} = \frac{BW}{(2\pi (f_c)^2 g_i Z_o} \tag{4}$$

where, n is the number of LC pairs,
i designate the order of the filter,
f_c gives the cut-off frequency,
BW is the pass band,
Z_o is the transmitting side impedance
g_i is the immittance of the circuit

A 3rd order Butterworth band pass filter, shown in Fig. 4, has been designed and simulated first limiting the number of LC pairs to two. The objective is to identify the performance that can be achieved when such theoretically calculated ideal values are used. The theoretical values, shown in Table 1, were calculated using using Eqs. (1) to (4) and adapted in the circuit configuration below.

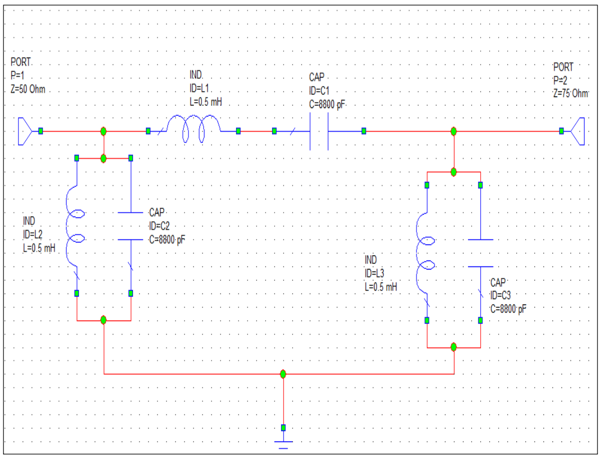

Fig. 4. 3rd order Butterworth band pass filter

For analyzing the frequency response of the Butterworth circuit, the cut-off frequency was chosen as 100 kHz because it allows the Butterworth filter passband cover the CENELEC band of frequencies. The strength of PLC signal will be highest around 100 kHz and the insertion loss is expected to be lowest at the cut-off frequency. Two different LC pair combinations were used to evaluate this circuit. The first one is a standard power line to modem (with a 50 Ω/75 Ω impedance ratio) with the theoretical LC component values given in Table 1. The second one is a similar circuit, where the same impedance ratio has been used with practically available LC off-the-shelf component values.

TABLE 1. LIST OF THE THEORETICAL VALUE OF THE COMPONENTS FOR STANDARD 50 Ω/75 Ω IMPEDANCE COMBINATIONS

Parameters	**Values**
L_{series}	0.5 mH
L_{shunt}	0.5 mH
C_{series}	8800 pF
C_{shunt}	8800 pF

Fig. 5 shows the insertion loss graph for the first circuit with theoretical values. The insertion loss graph shows that if theoretically calculated values are used, the circuit would give an almost perfect response. For example, in this particular case, the insertion loss is under -3 dB band in the 55 kHz to 160 kHz range. This implies that by setting circuit components to the theoretically obtained values, a very good CC may be obtained, with minimum attenuation of the PLC signals.

But, the required capacitance and inductance values are not practical and not commercially available.

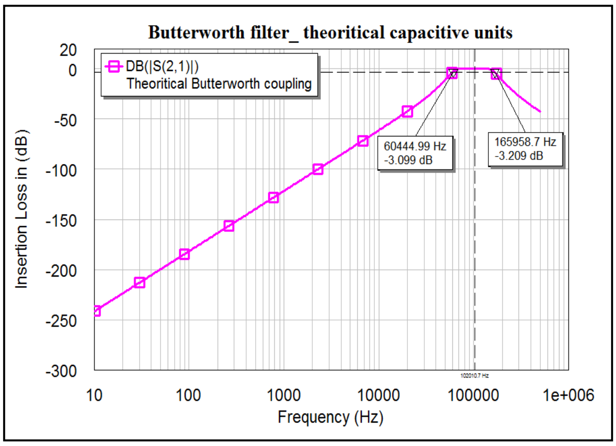

Fig. 5 Insertion Loss graph for (50/75) Ω theoretical Butter worth coupling circuit

Many researchers [18, 20] in the literature assume such theoretically calculated practical values in their designs. This work aims to target this shortcoming by demonstrating how good responses could still be obtained by using commercially available off-the-shelf components. Therefore, in the second part of the simulation, the theoretically obtained component values were changed to practically available values, ratings of which are given in Table 2. As shown in Table 2, capacitance has been chosen as 8800 pF, which is a very common value capacitor that is commercially manufactured by ABB electronics. Similarly, the value of the inductance has been chosen as 0.5 mH, which is also commercially available.

TABLE 2. LIST OF THE PRACTICALLY AVAILABLE COMPONENTS FOR STANDARD 50 Ω/75 Ω IMPEDANCE COMBINATIONS

Parameters	**Values**
L_{series}	159154.943 nH
L_{shunt}	79577.472 nH
C_{series}	15915.494 pF
C_{shunt}	31830.989 pF

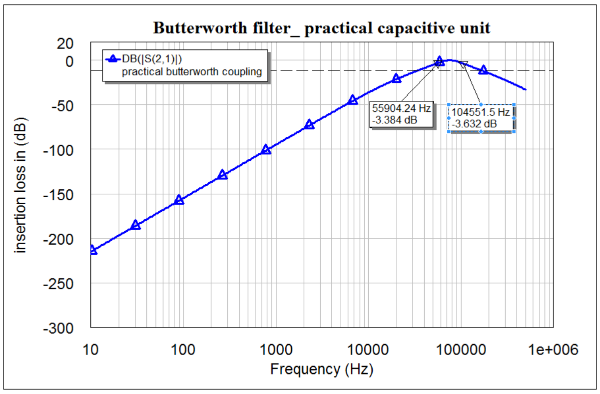

Fig. 6 Insertion Loss graph for (50/75) Ω practical Butter worth coupling circuit

The insertion loss graph of the modified circuit is shown in Fig. 6. As shown, for the lower part of the CENELEC band, this circuit produces a very high insertion loss more than -53 dB, but from 55 kHz to 100 kHz, the insertion loss is very low (less than -3 dB) which is very promising for use in real-time PLC applications over power networks. Even though the designed circuit will not be adequate in the 9 kHz to 55 kHz range, its insertion loss performance will be quite ample in the 55 kHz to 100 kHz range. This result validates the feasibility of using the practical Butterworth filter as a coupling arrangement for real world PLC applications.

IV. MODELLING OF WIDE BAND LINE TRAP CIRCUIT

Different types of LT circuits such as band-stop, the notch filter, wide-band LC resonant and the T-type filter circuits can be used as the LT circuit. However, amongst them, the T-type LT circuit is the most widely used according to the literature. Most LT circuits have been designed and modelled to isolate signals over 1 MHz in high frequency data communications applications. In the previous section, a Butterworth filter based CC was designed to operate with minimum attenuation in the 55 kHz to 100 kHz frequency band. In this section, the objective is on designing a LT circuit that would block frequencies in this range. Fig. 7 and Fig. 8 show the circuit diagrams of the single stage and double stage T-type LT circuits, appropriate for power system networks.

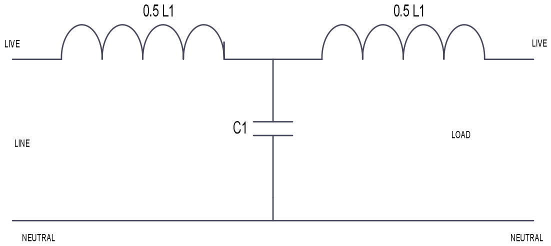

Fig. 7 Single stage T-type line trap circuit

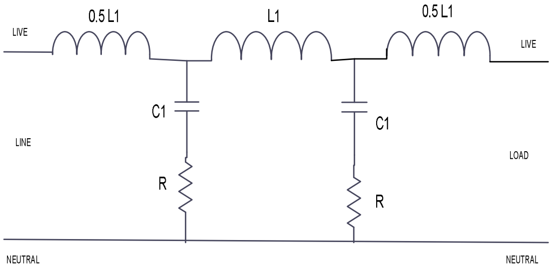

Fig. 8 Double stage line trap circuit

Eqs. (5) to (6) are the fundamental equations [20] that can be used to calculate any ratio such as the S-parameters, gain and etc. associated with LT circuits.

$$\begin{bmatrix} V_{in} \\ I_{in} \end{bmatrix} = \begin{bmatrix} 1 & \dfrac{jkR_d}{2} \\ 0 & 1 \end{bmatrix} \begin{bmatrix} 1 & 0 \\ \dfrac{jk}{R_d} & 1 \end{bmatrix} \begin{bmatrix} 1 & \dfrac{jkR_d}{2} \\ 0 & 1 \end{bmatrix} \begin{bmatrix} V_{out} \\ I_{out} \end{bmatrix} \qquad (5)$$

$$\Rightarrow \begin{bmatrix} V_{in} \\ I_{in} \end{bmatrix} = \begin{bmatrix} \dfrac{2-k^2}{2} & \dfrac{jkR_d}{4}(4-k^2) \\ \dfrac{jk}{R_d} & \dfrac{2-k^2}{2} \end{bmatrix} \begin{bmatrix} V_{out} \\ I_{out} \end{bmatrix} \qquad (6)$$

Where, J is an imaginary term,
R_d is the filter design impedance,
K is the normalized frequency defined by the trouble frequency F and cut off frequency F_C as in Eq. (7)

$$k = \frac{F_C}{F} \qquad (7)$$

Using the Eqs. (5) to (6), frequency co-relation between any types of LT circuits can be modelled. For this work, a double-stage T-type LT circuit has been modelled and evaluated with the same practical LC components that were used in building the CC stages. These include the 8800 pF capacitance and the 50 mH inductance.

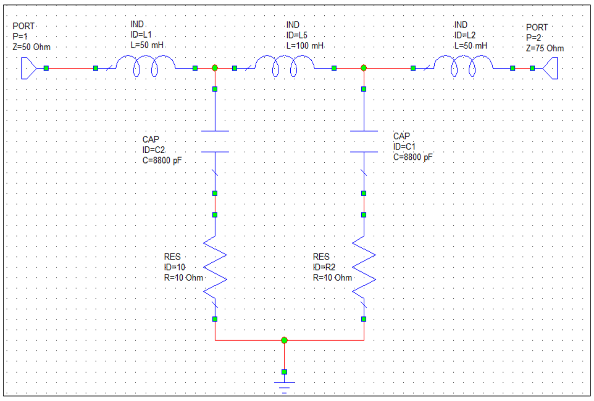

Fig. 9 Double stage T- type line trap circuit in Microwave window view

Fig. 9 shows the Microwave Office design view of the LT circuit that has been modeled using commercially available capacitive and inductive components. The insertion loss of the designed circuit is shown in Fig. 10.

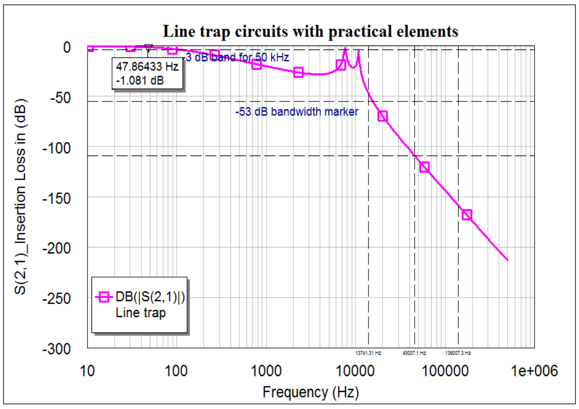

Fig. 10 Insertion loss graphs of the line trap circuit

The results demonstrate that the circuit permits the power signal (50 Hz) with a low attenuation (< -3 dB) and for the CENELEC band of frequencies, the circuit produces high insertion losses. Specifically, for frequencies above 55 kHz, this circuit provides a large attenuation more than -53 dB. This design would therefore ensure that the LT will block PLC signals in the 55 kHz to 100 kHz range from penetrating into areas of the network where generating units may be present.

V. DISCUSSION

A comparative discussion of the LT vs. CC is presented in this Section. Fig. 11 plotted to show the comparative insertion loss curves for both circuits. The pink curve is for the Butterworth CC circuit, where the peak of the insertion curve lies on the 55 kHz to 100 kHz range, and the insertion loss in this range is less than -3 dB. The blue curve is for the LT circuit, which exhibits very high insertion loss (larger than -53 dB) in the same band. The results achieved confirm that these two circuits can be used in power system PLC applications where the frequency of the PLC signal must be chosen between 55 kHz to 100 kHz.

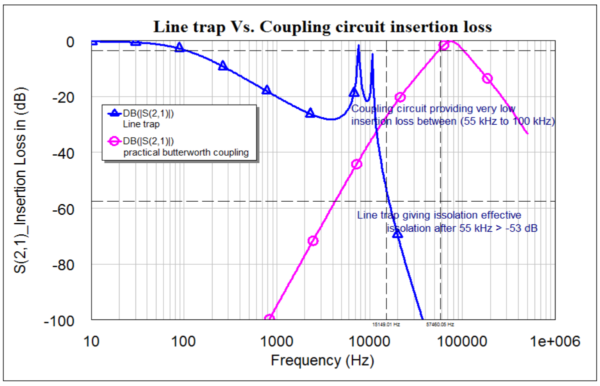

Fig. 11 Insertion loss graphs for the LT vs. practical Butterworth CC

VI. CONCLUSION

In this paper, a Butterworth type CC and a T-type LT circuit have been modelled, simulated and evaluated for use in power system applications where the PLC signal frequency is to be selected within the CENELEC frequency band. The circuits were designed using commercially available off-the-shelf components. The insertion loss of the CC was measured as -3 dB in the 55 kHz to 100 kHz range, and the insertion loss of the LT was measured as more than -53 dB. Therefore, sufficient performance was achieved in terms of insertion loss profile of the circuits. This shows that if the PLC signal transmission frequency can be chosen within the 55 kHz to 100 kHz portion of the CENELEC frequency range, then the designed circuits can be perfectly used in real-time applications.

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