Design and Performance Analysis of a CMOS Amplifier for Ultra-Wide Band Wireless Receivers Using Substrate Integrated Waveguide Resonator

By

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Declaration

I hereby declare that the work contained in this thesis has not been previously submitted to meet requirements for an award at this or any other higher education institution. To the best of my knowledge and belief, the thesis contains no material previously published or written by another person except where due reference is cited.

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List of Publications

Conference

- Publication 1: M. M. H. Tareq, N. Jahan and Q. D. Hossain, "Design of a Millimetre-wave Band LNA Using SIW Resonator in 180-nm CMOS Technology," 2023 6th International Conference on Electrical Information and Communication Technology (EICT), Khulna, Bangladesh, 2023, pp. 1-5, Doi: 10.1109/EICT61409.2023.10427849.

- Publication 2: M. M. H. Tareq, N. Jahan and Q. D. Hossain, "Enhancing Low Noise Amplifiers: A Comparative Study of Substrate Integrated Waveguide Resonators and Traditional Inductors in 180 – nm CMOS Technology" (Under processing)

Approval by the Supervisor

This is to certify that **Mohammad Mahmudul Hasan Tareq** has carried out this work under my supervision, and that he has fulfilled relevant Academic Ordinance of the Chittagong University of Engineering and Technology, so that he is qualified to submit the following thesis in application for the degree of M.Sc. in EEE.

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I am truly grateful to everyone who has played a part, directly or indirectly, in the completion of my M.Sc. thesis.

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Abstract

This research introduces a novel approach to the design of an ultra-wideband (UWB) low noise amplifier (LNA) by leveraging the substrate integrated waveguide (SIW) resonator. The proposed inductor less LNA operates in the frequency range of 67.5 GHz to 71.5 GHz, strategically aligning with the 180 nm technology transition frequency (fT). The distinct high-quality factor (Q) characteristic inherent in SIW resonators is harnessed to achieve a commendable gain ($|S_{21}|$) at the designated operating frequencies.

Central to the advancement of this LNA design is the seamless integration of SIW resonators, a departure from conventional approaches employing active spiral inductors. This departure marks a pioneering effort in the application of SIW in complementary metal-oxide-semiconductor (CMOS) LNA design, thereby eliminating the need for active spiral inductors and opening new avenues for enhanced performance.

To further enhance the noise performance of the LNA, a sophisticated noise canceller circuit is introduced. This integrated common source and common gate topology, intricately blended with the original common gate configuration, significantly contributes to noise reduction. The judicious incorporation of the noise canceller circuit not only maintains an excellent input match ($|S_{11}| < -14$ dB) and output match ($|S_{22}| < -15$ dB) but also contributes to an average noise figure of 8.3 dB and a power gain of 9.76 dB at 69 GHz.

The significance of this work extends beyond the mere introduction of an inductor-less SIW-based LNA. The utilization of SIW resonators brings forth a technological milestone in CMOS LNA design. By eliminating the active spiral inductor, the proposed LNA achieves a delicate balance between gain, noise performance, and frequency compatibility. This research represents a breakthrough, opening new avenues for the application of SIW in high-frequency electronics and advancing the frontiers of CMOS LNA design.

In conclusion, this study not only presents a technologically innovative inductor-less SIW-based UWB LNA but also underscores the potential of SIW resonators in revolutionizing the landscape of CMOS LNA design. The findings contribute to the ongoing discourse in high-frequency electronics and pave the way for further exploration and refinement in future research endeavours.

সারাংশ

এই গবেষণাটি সাবস্ট্রেট ইন্টিগ্রেটেড রেজোনেটর ব্যবহারের মাধ্যমে লো-নয়েজ অ্যামপ্লিফায়ার ডিজাইনের একটি ব্যতিক্রমধর্মী প্রচেষ্টা সম্পর্কে ধারণা দেয়। ১৮০ ন্যানোমিটার প্রযুক্তির সাথে সামঞ্জস্যপূর্ণ প্রস্তাবিত এই ইন্ডাক্টর-বিহীন লো-নয়েজ অ্যামপ্লিফায়ারটি ৬৭.৫ থেকে ৭১.৫ গিগাহার্টজ কম্পাংক সীমার ভেতরে কাজ করে। সাবস্ট্রেট ইন্টিগ্রেটেড রেজোনেটর এর সহজাত উচ্চ কোয়ালিটি ফ্যাক্টরকে কাজে লাগিয়ে উপরোক্ত কম্পাংক সীমার মধ্যে উল্লেখযোগ্য বিবর্ধন অর্জন করা হয়েছে।

এই লো-নয়েজ অ্যামপ্লিফায়ার ডিজাইনের মূল বিষয় হলো সাবস্ট্রেট ইন্টিগ্রেটেড রেজোনেটর এর নিখুঁত ব্যবহার, যেটি ইন্ডাক্টর ব্যবহারকারী গতানুগতিক ডিজাইনগুলো থেকে ব্যতিক্রমধর্মী। এই লো-নয়েজ অ্যামপ্লিফায়ারটি কমপ্লিমেন্টারি মেটাল অক্সাইড সেমিকন্ডাক্টর এ লো-নয়েজ অ্যামপ্লিফায়ার ডিজাইনের ক্ষেত্রে সাবস্ট্রেট ইন্টিগ্রেটেড রেজোনেটর এর প্রয়োগের একটি যুগান্তকারী প্রচেষ্টা, যার ফলে ইন্ডাক্টর ব্যবহারের প্রয়োজন ফুরোবে এবং আরও ভালো ফলাফলের নতুন দিগন্ত উন্মোচিত হবে।

এই লো-নয়েজ অ্যামপ্লিফায়ারটির নয়েজের ফলাফল আরও উন্নত করতে একটি জটিল নয়েজ কেন্সেলার সার্কিটের ধারণা দেয়া হয়েছে। কমন গেইট কনফিগারেশনের সাথে সূক্ষভাবে মিশ্রিত এই ইন্টিগ্রেটেড কমন সোর্স এবং কমন গেইট পদ্ধতিটি নয়েজ কমাতে উল্লেখযোগ্য ভূমিকা পালন করে। নয়েজ কেন্সেলার সার্কিটটির এই সুচিন্তিত ব্যবহার কেবল অসাধারণ ইনপুট ম্যাচিং ($এস_{১১}$<— ১৪) এবং আউটপুট ম্যাচিং ($এস_{২২}$<— ১৫) ই বজায় রাখে না, উপরন্তু ৬৯ গিগাহার্টজ কম্পাংকে গড়ে নয়েজ ফিগার এর মান ৮.৩ ডেসিবল এবং পাওয়ার গেইন ৯.৭৬ ডেসিবল রাখতে সহায়তা করে।

এই গবেষণার তাৎপর্য হল ইন্ডাক্টরবিহীন সাবস্ট্রেট ইন্টিগ্রেটেড রেজোনেটর ভিত্তিক লো-নয়েজ অ্যামপ্লিফায়ার-এর সাথে পরিচিত করা। কমপ্লিমেন্টারি মেটাল অক্সাইড সেমিকন্ডাক্টর এ লো-নয়েজ অ্যামপ্লিফায়ার ডিজাইনে সাবস্ট্রেট ইন্টিগ্রেটেড রেজোনেটর এর ব্যবহার প্রযুক্তিগত মাইলফলক বয়ে আনবে। ইন্ডাক্টর এর প্রয়োজনীয়তাকে দূর করার মাধ্যমে প্রস্তাবিত লো-নয়েজ অ্যামপ্লিফায়ারটি গেইন, নয়েজ এবং কম্পাংক এর মাঝে সামঞ্জস্য বজায় রাখতে সক্ষম হবে। এই গবেষণাটি উচ্চ কম্পাংক ইলেক্ট্রনিক্সের ক্ষেত্রে সাবস্ট্রেট ইন্টিগ্রেটেড রেজোনেটর প্রয়োগের ক্ষেত্রে একটি মাইলফলক, যা উন্মোচন করবে নতুন সম্ভাবনার দ্বার এবং কমপ্লিমেন্টারি মেটাল অক্সাইড সেমিকন্ডাক্টর এ লো-নয়েজ অ্যামপ্লিফায়ার ডিজাইনের ক্ষেত্রে অগ্রপথিক হিসেবে ভূমিকা রাখবে।

পরিশেষে, এই গবেষণাটি কেবল প্রযুক্তিগতভাবে নতুন এবং ব্যতিক্রমধর্মী একটি ইন্ডাক্টর-বিহীন সাবস্ট্রেট ইন্টিগ্রেটেড রেজোনেটর ভিত্তিক আল্ট্রা ওয়াইড ব্যান্ড সম্পন্ন লো-নয়েজ অ্যামপ্লিফায়ার-এর ধারণাই দেয় না বরং কমপ্লিমেন্টারি মেটাল অক্সাইড সেমিকন্ডাক্টর এ লো-নয়েজ অ্যামপ্লিফায়ার ডিজাইনের ক্ষেত্রে সাবস্ট্রেট ইন্টিগ্রেটেড রেজোনেটর এর গুরুত্বকেও তুলে ধরে। এই গবেষণালব্ধ ফলাফল চলমান উচ্চ কম্পাংক ইলেক্ট্রনিক্সের গবেষণায় নতুন সংযোজন হবে এবং ভবিষ্যতে আরও নতুন নতুন গবেষণার ক্ষেত্রে পথপ্রদর্শক হিসেবে কাজ করবে।

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List of Symbols

Q	Quality Factor
dB	Decibel
P_{s_in}	Input Signal Power
P_{n_in}	Input Noise Power
P_{s_out}	Output Signal Power
P_{n_out}	Output Noise Power
K	Boltzmann's Constant
T	Temperature In Kelvin
Δf	Bandwidth
Hz	Hertz
g_{d0}	Drain to Source Conductance
ρ_{sh}	Silicide Sheet Resistance
W	Width of MOSFET
L	Length of MOSFET
ρ_{con}	Polysilicon Contact Resistance
Si	Silicon Substrate
SiO_2	Silicon di-Oxide
C_{ox}	Gate Oxide Capacitance Per Unit Area
I_{DC}	DC Current
g_m	Transconductance
GHz	Giga Hertz
mW	Milli-Watt
mm	Millimetre
μm	Micrometre

P_h	Distance Between Vias
D_m	Diameter of Via
λ_g	Guided Wavelength
c	Velocity of Light in the Vacuum
f_r	Design Frequency
Ω	Ohm
nm	Nanometre

List of Abbreviations

UWB	Ultra-Wide Band
WPANs	Wireless Personal Area Networks
OP-AMPs	Operational Amplifiers
GBW	Gain Bandwidth
SIW	Substrate Integrated Waveguide
RF	Radio Frequency
LNA	Low Noise Amplifier
NF	Noise Figure
SNR	Signal to Noise Ratio
BJTs	Bipolar Junction Transistors
FETs	Field Effect Transistors
IIP3	Third order Input Interception Point
CS	Common Source
CG	Common Gate
NMOS	N-type Metal Oxide Semiconductor
PMOS	N-type Metal Oxide Semiconductor
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
DA	Distributed Amplifier
DGS	Defected Ground Structure
FB	Feed Back
MOS	Metal Oxide Semiconductor
PSD	Power Spectral Density

1 Introduction

1.1 Background

During this period of rapid technological growth, the technology of wireless communication plays an essential part in the connections that are made in the modern world. From mobile devices to applications for the Internet of Things, it is becoming increasingly important for a wide variety of devices to have the ability to transfer data effectively and communicate without any interruptions. The tremendous bandwidth capacity of Ultra-Wide Band (UWB) technology makes it a promising alternative for handling the growing demand for broadband internet.

UWB technology has expanded beyond its initial application in radar systems to embrace a variety of different areas, including healthcare, automobile radar, accurate indoor location services, and wireless personal area networks (WPANs). One of the most notable characteristics of UWB is its capacity to transmit data over a broad bandwidth, which enables high transmission speeds and an accurate tracking of location.

1.2 Motivation

UWB technology shows promise but comes with specific challenges, particularly in signal amplification. UWB signals necessitate amplifiers with exceptional bandwidth to operate effectively over a broad frequency range due to their vast frequency range. Designing and implementing amplifiers in UWB systems is made more complex by the need for low noise figure and high linearity. Figure 1.1 depicts the use of UWB in various applications.

Figure 1.1: Applications of UWB [1]

Traditional amplifier designs often do not meet the high-performance requirements of UWB communication due to being optimized for narrower bandwidths. Achieving the challenging technical task of balancing bandwidth, gain, and noise performance requires innovative ideas and advanced technology.

1.2.1 Operational Amplifiers (OP-AMPs) in UWB Systems

Operational Amplifiers (OP-AMPs) play a vital role in signal amplification and conditioning in electronic systems, including UWB communication systems. Designing OP-AMPs for UWB applications poses specific challenges due to the wide frequency range, high gain requirements, and stringent performance specifications. Traditional OP-AMP designs struggle to achieve the desired bandwidth, gain, power consumption, and noise performance necessary for UWB systems.

The design of operational amplifiers for UWB systems requires careful consideration of several factors. One of the main challenges is achieving a wide bandwidth to accommodate the UWB frequency range. Traditional OP-AMP designs often struggle to achieve the necessary gain-bandwidth product (GBW) for UWB applications. Researchers have explored various approaches to overcome this limitation, including the use of multi-stage amplification, distributed amplifiers, and active inductors. Figure 1.2 illustrates the operation and basic symbol of an operational amplifier (Op-amp).

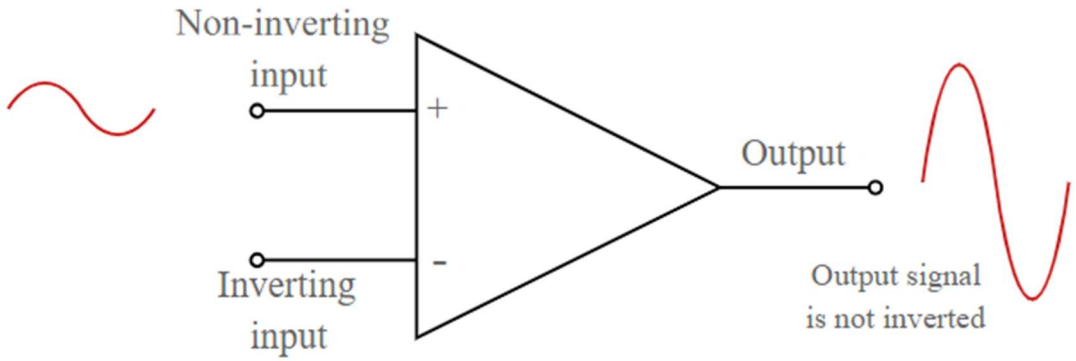

Figure 1.2: Basic symbol of an Op-amp [2]

Another critical consideration is the power consumption of the OP-AMP. UWB systems typically require low-power operation to extend battery life and ensure energy efficiency. Design techniques such as biasing optimization, adaptive biasing, and subthreshold operation have been investigated to minimize power consumption while maintaining acceptable performance.

Additionally, UWB OP-AMPs must exhibit low noise characteristics to preserve the signal integrity and achieve high data rates. Noise optimization techniques, such as noise figure matching, input transistor sizing, and proper biasing, have been explored to mitigate noise contributions and improve overall system performance.

1.2.2 The Prospects of Substrate Integrated Waveguide (SIW) Resonators

The advancement of Substrate Integrated Waveguide (SIW) resonators is a crucial progression in achieving efficient Ultra-Wideband (UWB) expansion. Their unique characteristics, including a high-quality factor (Q-factor) and compatibility with integrated circuit technology, make them an attractive choice for enhancing amplifier performance. Incorporating substrate integrated waveguide (SIW) resonators into the operational amplifier (OP-AMP) design enables achieving high bandwidth, gain, and low noise performance, offering a ground breaking solution to ultra-wideband (UWB) amplification challenges. Fabricated SIW for mm-waveband application is shown in figure 1.3.

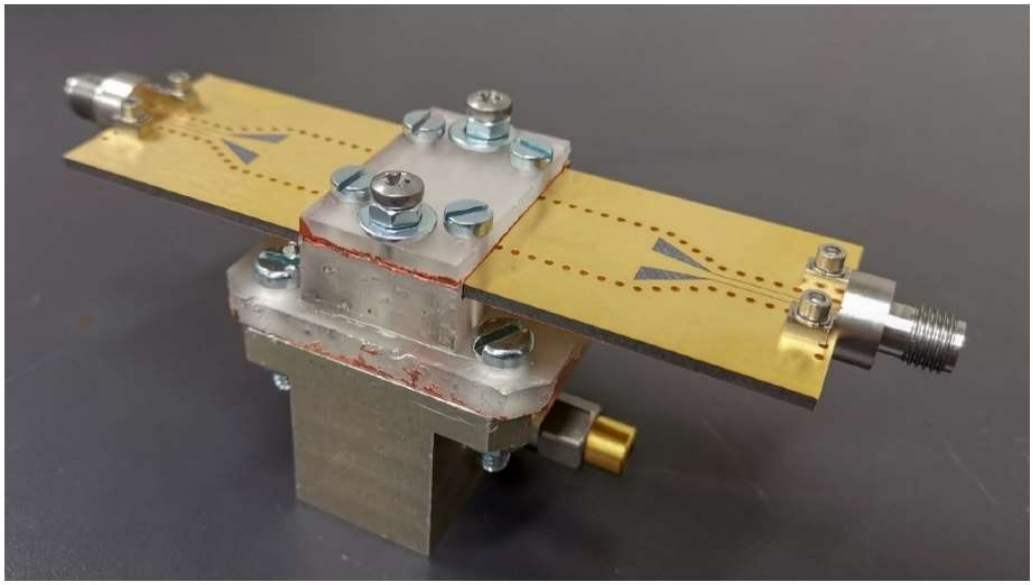

Figure 1.3: Fabricated SIW Resonator [3]

1.2.2.1 Planar Structure and Wave Propagation

Provide a detailed explanation of the planar structure of SIW, discussing its fabrication techniques and advantages in terms of miniaturization and ease of integration. Elaborate on guided wave propagation within SIW, emphasizing the confinement of signals within the substrate, reducing radiation losses, and enhancing efficiency.

1.2.2.2 Resonance in SIW

Delve into the physics of resonance in SIW resonators, exploring how the electromagnetic waves interact within the structure to create resonant modes. Discuss the role of parameters such as the width and height of the SIW in determining the resonant frequency, providing a more in-depth understanding.

1.2.2.3 High-Quality Factor (Q-factor)

Define Q-factor in the context of resonators, explaining its role in determining the sharpness of the resonance peak and signal quality. Provide examples of how the high Q-factor of SIW resonators leads to longer ring-down times and better energy storage, crucial for applications demanding signal integrity.

1.2.2.4 Compatibility with Integrated Circuit Technology

Elaborate on the compatibility of SIW resonators with integrated circuits, discussing the fabrication processes involved and the advantages of co-integration. Explore specific examples of successful integration, showcasing the versatility of SIW resonators in various circuit designs. Provide a nuanced understanding of how SIW resonators contribute to radar system performance, considering applications like automotive radar or advanced surveillance. Discuss improvements in range resolution, target discrimination, and overall radar sensitivity.

1.2.2.5 Enhancements in Bandwidth and Gain

Detail how the integration of SIW resonators extends the bandwidth of OP-AMPs, breaking down the technical aspects of bandwidth enhancement through resonator coupling. Discuss the trade-offs involved in gain enhancement, including the consideration of power consumption and stability. Showcase specific wireless communication scenarios where SIW resonators are instrumental, such as in 5G or beyond-5G applications. Discuss the impact on signal coverage, interference mitigation, and the potential for increased data

transfer rates. Explore the intricacies of SIW resonators in biomedical applications, including their role in medical imaging systems, implantable devices, or wireless healthcare monitoring.

1.2.2.6 Noise Reduction

Provide an in-depth analysis of how SIW resonators contribute to noise reduction in OP-AMPs, considering the impact on signal-to-noise ratio (SNR) and overall system performance. Explore design strategies and methodologies employed to achieve optimal noise performance.

Conduct a thorough analysis of current challenges in SIW resonator technology, addressing issues such as manufacturing tolerances, frequency agility, or material limitations. Consider the impact of environmental factors on SIW resonator performance and reliability. Emphasize the transformative impact on amplifier performance, signalling a paradigm shift in addressing UWB amplification challenges.

1.2.3 LNA Fundamental

In the field of radio frequency (RF) and microwave engineering, a Low Noise Amplifier, often known as an LNA, is an essential component. Increasing the strength of weak signals while simultaneously introducing as little noise as possible is its major purpose. In communication systems, low-noise amplifiers (LNAs) serve a crucial function, particularly in situations when the signal that is received is weak. Examples of such situations include wireless receivers and satellite communications services. When it comes to building and optimizing amplifiers for a variety of applications, having a solid understanding of the fundamental concepts of LNAs is absolutely necessary.

1.2.4 Importance of Low Noise

When it comes to the complex landscape of amplifier design, the defining characteristic of a Low Noise Amplifier (LNA) is that it has an uncompromising emphasis on achieving low noise performance. Because of this distinguishing

feature, low-noise amplifiers (LNAs) are considered to be vital components, particularly in communication systems, where the fidelity of the signals that are received is automatically vulnerable to a wide variety of problems.

1.2.4.1 Inherent Weakness of Received Signals

Among the many challenges that are encountered in the field of communication systems, one of the most common ones is the inherent fragility of received signals. This vulnerability can be attributable to a wide variety of variables, including the weakening of signals across long distances, the detrimental effects of interference, and the utilization of low-power transmitters. These factors all contribute to the fragility of the structure. When all of these elements come together, the result is a situation in which the incoming signal is not just weak but also susceptible to disturbances from the outside world.

1.2.4.2 Noise Figure and Noise Temperature

There are two metrics that are commonly used to quantify the performance of an LNA. These parameters are known as the noise figure (NF) and the noise temperature (T). The noise figure indicates the performance of an amplifier by comparing its actual noise output to the theoretical minimum noise output, known as the quantum limit. A lower noise figure demonstrates improved performance. On the other hand, noise temperature is a measurement of the amount of thermal noise power that the amplifier contributes to the system. Characterizing noise performance is made easier by the fact that it is stated in Kelvin (K), which is a unit of measurement.

1.2.4.3 Preservation of Signal Integrity

In such scenarios, the necessity for achieving high levels of noise reduction in amplifiers, particularly in low noise amplifiers (LNAs), becomes critically significant. Not only is the amplification of the signal the primary objective, but also the maintenance of the signal's integrity. When it comes to protecting the signal-to-noise ratio (SNR), which is a fundamental measure that defines the

quality of the information that is received, the delicate interaction that occurs between the frequency of the signal and the noise becomes a critical determining factor.

1.2.4.4 Signal-to-Noise Ratio (SNR) Considerations

One of the most important parameters to consider when evaluating the robustness of a communication system is the Signal-to-Noise Ratio, often known as SNR. When the signal-to-noise ratio (SNR) is high, it indicates that the ability to differentiate between signal and noise is higher, which directly translates into improved signal clarity. This delicate equilibrium is put in jeopardy when extra noise is introduced during the process of amplification, which has the potential to compromise the signal's ability to be discerned amidst the background noise.

When it comes to signal amplification, a cautious approach is required because of the inherent fragility of weak signals. Any increase in noise levels that occurs throughout this process has the potential to cause a decrease in the signal-to-noise ratio (SNR), which can then have a domino effect on the overall quality of the information that is received. The reduction in the quality of the information is not only a theoretical worry; rather, it is a concrete result that has implications for the efficiency of the entire communication system.

Because of their dedication to reducing noise, local noise abatement systems (LNAs) have emerged as entities that play an important role in this context. Finding the ideal balance between signal amplification and noise reduction is one of the painstaking design concerns that are inherent in low-noise amplifiers (LNAs). Through the application of advanced engineering, low-noise amplifiers (LNAs) strive to amplify weak signals with the highest possible efficiency while introducing the least amount of additional noise possible. This helps to ensure that the information that is received is accurate and reliable.

1.2.5 Gain and Bandwidth

Gain and bandwidth are crucial factors in determining the effectiveness and performance of a Low Noise Amplifier (LNA) in amplifier design. An LNA's primary function is to minimize noise while also amplifying weak input signals and offering a wide bandwidth to support various frequency ranges in modern communication systems.

The primary function of an LNA is to provide adequate gain. Gain, defined as the ratio of output signal power to input signal power and commonly represented in decibels (dB), is a crucial element in the amplification process. It coordinates the conversion of faint input signals into clear and powerful entities, making them suitable for smooth advancement through following phases in the communication system. Adjusting signal strength with precision through gain is crucial for maintaining signal accuracy throughout transmission despite various challenges.

Gain in amplifier design represents more than just a numerical value; it signifies how efficiently and effectively an LNA increases the strength of incoming signals. Choosing the right gain parameters during the design process is crucial as it determines the trade-off between signal amplification and the risk of adding unwanted noise. This fragile balance showcases the precise engineering needed to attain the best amplification results.

The bandwidth of a Low Noise Amplifier (LNA) is a crucial factor that affects its operational range in addition to the need for profit. Bandwidth refers to the range of frequencies within which the LNA may operate well without any noticeable decrease in performance. In the vast field of modern communication systems, which have various frequency allocations and strict requirements for signal quality across the entire range, the bandwidth of an LNA is a crucial element.

A carefully chosen bandwidth allows for effective signal amplification within a specific frequency range and provides the ability to adjust to changing frequencies. The versatility and application of an LNA in many situations are highlighted by its capability to navigate complex frequency networks in real-world communication scenarios.

The combination of gain, bandwidth, and low noise performance represents the complex balancing required in LNA design. Engineers carefully balance several factors to design an amplifier that efficiently amplifies weak signals and functions smoothly across a specific frequency range. Optimizing gain and bandwidth while maintaining low noise is the epitome of engineering perfection in LNA development.

1.2.6 Transistor Selection and Biasing

Transistor technology selection and precise biasing method are crucial elements in Low Noise Amplifier (LNA) design. Choosing between transistor types like Bipolar Junction Transistors (BJTs) and Field-Effect Transistors (FETs) requires careful evaluation of their specific benefits and drawbacks.

BJTs are well-known for their linearity and strong transconductance, making them ideal for applications that require linear amplification. On the other hand, FETs are favoured in situations where noise performance is more important due to their high input impedance and lower noise figures. Effective decision-making requires a deep comprehension of the application context and a thorough assessment of performance metrics.

The biasing technique functions as a conductor in this orchestration, establishing the best operating points to maintain a precise equilibrium between linearity, gain, and noise performance. Optimal linearity is achieved by managing non-linearities by precise biasing, maintaining signal integrity, and reducing distortions. Regulating gain is closely connected to fine-tuning

accuracy, guaranteeing the amplifier functions within the intended range for the best amplification.

1.2.7 Matching Networks and Impedance Matching

In amplifier design, matching networks play a crucial role by aligning the input and output impedances of the Low Noise Amplifier (LNA) with surrounding components and transmission lines. Precise alignment is crucial to maximize power transfer efficiency and reduce signal reflections in the system. Matching networks are crucial for establishing smooth connectivity between the LNA and its external surroundings. They help maintain a balanced signal flow and reduce impedance differences that may affect the amplifier's performance. The careful use of these networks is crucial in amplifier engineering, significantly enhancing the effectiveness and dependability of the LNA.

Matching networks in LNAs play a crucial role in improving power transfer and reducing signal reflections, which strengthens the amplifier's performance in a communication system. Intentional impedance matching is not just a technical detail but a fundamental approach for achieving the best amplifier performance. Engineers use exact matching networks to incorporate an LNA into its operational environment, resulting in an amplified signal with maximum quality and efficiency. Impedance matching is a crucial discipline in amplifier design that demonstrates a dedication to technical precision for optimal amplifier performance.

1.2.8 Stability and Linearity

Stability is a crucial factor in Low Noise Amplifier (LNA) design to prevent unwanted oscillations or instabilities. Engineers use feedback networks and stabilize components to strengthen the LNA and ensure its reliable operation in the communication system. Ensuring stability is crucial in LNA engineering to prevent any negative impacts on the amplifier's dependability and performance.

The idea of linearity is crucial in LNA design, as it determines the amplifier's capacity to accurately replicate input signals without distorting them. This quality is especially important in situations where the LNA deals with strong interfering signals. Maintaining good linearity is crucial to prevent signal degradation and preserve signal integrity. Striving for excellent linearity in LNA design showcases a dedication to engineering precision. The amplifier's ability to faithfully replicate input signals, especially under difficult circumstances, highlights its importance as a crucial component in advanced communication systems.

1.2.9 Power Consumption

In the complex field of Low Noise Amplifier (LNA) design, achieving low noise and high gain is crucial, but balancing power consumption is also important, especially in situations with limited energy resources like battery-powered devices. Balancing low noise, high gain, and power efficiency requires precise design strategies to optimize power consumption while maintaining important noise performance. It is crucial to maintain a careful balance in real LNA implementations to achieve high efficiency while ensuring optimal noise characteristics. This balance is necessary to overcome the problems given by energy limits in different applications.

A comprehensive comprehension of LNA basics goes beyond only focusing on low noise and high gain, encompassing a wide range of factors. This thorough analysis covers important factors like noise figure, bandwidth, transistor choice, and biasing, all of which have a unique impact on the performance of the LNA. Careful coordination of impedance matching, strategic stability control, and maintaining linearity are other complexities in this complicated design. The importance of power consumption is significant and requires a balanced approach to enhance energy efficiency while maintaining low noise and achieving substantial gain.

To master LNA design, one must combine these complex ideas. It requires a deep understanding of low noise, gain, noise figure, bandwidth, and the intricate relationship between transistor technology and biasing. Implementing impedance matching, ensuring stability, and maintaining linearity are important design considerations. This expertise goes beyond the usual limits to include a complex comprehension of power usage, recognizing its vital importance in contemporary, energy-efficient uses. Mastering these concepts enables engineers to customize LNAs precisely, guaranteeing their smooth incorporation into particular applications and reinforcing their position as strong performers in communication systems.

1.3 Objective of the Thesis

The primary objectives of this thesis are:

1. To design Substrate Integrated Waveguide (SIW) Resonator for required resonance frequency.
2. To design a Low Noise Amplifier (LNA) for Ultra-Wide Band (UWB) wireless receiver using SIW Resonator.
3. To explore the performance of the proposed LNA

Through the pursuit of these objectives, this thesis endeavours to contribute to the advancement of UWB communication systems by providing an innovative approach to Ultra-Wide Band OP-AMP design using SIW resonators.

1.4 Significance and Scope

The significance of this research lies in its pioneering approach to the design of a wideband (WB) low-noise amplifier (LNA) using substrate integrated waveguide (SIW) technology. Traditional CMOS LNA design often relies on active spiral inductors, presenting challenges in achieving a delicate balance between gain, noise performance, and frequency compatibility. This study

introduces an innovative inductor-less SIW-based LNA, representing a ground-breaking departure from conventional methodologies. The seamless integration of SIW resonators not only eliminates the need for active spiral inductors but also opens new dimensions in high-frequency electronics, setting a technological milestone in CMOS LNA design.

The proposed LNA, operating in the 67 GHz to 71.5 GHz frequency range, aligns strategically with the 180 nm technology transition frequency, showcasing its relevance in contemporary technological landscapes. The incorporation of a sophisticated noise canceller circuit further enhances noise reduction, maintaining exceptional input and output matches. This research's significance extends beyond the immediate context, contributing to the ongoing discourse in high-frequency electronics and establishing new avenues for future exploration and refinement in CMOS LNA design.

The scope of this study encompasses the comprehensive exploration and implementation of SIW resonators in the design of a high-performance WB LNA. By focusing on the frequency range of 67 GHz to 71.5 GHz, the research addresses the specific challenges and opportunities associated with the 180 nm technology transition frequency. The investigation includes a detailed analysis of the inductor-less LNA's performance, the integration of SIW resonators, and the impact of the noise canceller circuit on key parameters such as gain, noise figure, and power gain. The study's scope extends to the broader implications of SIW technology in CMOS LNA design, emphasizing its potential to revolutionize high-frequency electronic systems.

1.5 Thesis Outline

Thesis is organized in five different chapters including this introduction chapter 1. In the introductory chapter of this thesis, we establish the foundation for a comprehensive study on the design and performance analysis of a CMOS amplifier tailored for ultra-wideband wireless receivers, with a specific focus on

the integration of a Substrate Integrated Waveguide (SIW) resonator. We outline the motivation behind this research, highlighting the significance of developing efficient amplifiers for improving wireless communication systems. Additionally, the chapter sets the stage for the subsequent analysis by presenting the objectives and scope of the study.

Chapter 2 delves into the fundamentals of Low-Noise Amplifiers (LNAs). It introduces readers to the essential concepts, operating principles, and key parameters governing the performance of LNAs. Additionally, a historical overview traces the evolution of LNA technology, providing a contextual foundation for the subsequent chapters.

A comprehensive overview of existing work in LNA design is presented in Chapter 3. The literature review summarizes relevant research, highlighting advancements, limitations, and emerging trends in LNA technology. By examining the current state of the field, this chapter provides a valuable context for the novel contributions of the present study.

Chapter 4 shifts focus to the design and optimization of Ultra-Wideband (UWB) LNAs. Readers are introduced to the unique characteristics of UWB LNAs and the design approach employed in this study. The chapter explores optimization techniques aimed at enhancing LNA performance, with a particular emphasis on the integration of Substrate Integrated Waveguide (SIW) technology.

The final chapter synthesizes the key findings of the research. It offers a concise summary of major contributions, discussing their implications and potential applications. Furthermore, the chapter outlines the scope for further research, identifying areas for exploration and refinement in the evolving field of LNA design.

2 Fundamentals of LNA

This chapter introduces the fundamental concept of S parameters, crucial for characterizing the behavior of two-port networks in RF circuits, with a particular focus on their application in optimizing Low Noise Amplifiers (LNAs) for wireless communication systems.

2.1 S Parameters

Instead of Z, Y, ABCD, and H parameters, the S parameter is frequently used to define two port networks when both networks are operating at RF frequencies. In terms of waves that are incident and waves that are reflected, the S parameters are defined. As can be seen in Figure 2.1, The waves that are incident and reflected at port_1 are denoted by x_1 and y_1, respectively. Similarly, the waves that are incident and reflected at port_2 are denoted by x_2 and y_2, respectively.

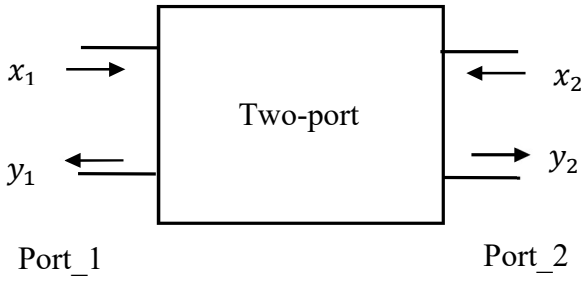

Figure 2.1: Two-port Network

The y_1 and y_2 are dependent on the x_1, x_2 and the delineation of the relationship between incident and reflected waves is explicated through the utilization of equations (2.1) and (2.2).

$$y_1 = S_{11}x_1 + S_{12}x_2 \quad (2.1)$$

$$y_2 = S_{21}x_1 + S_{22}x_2 \quad (2.2)$$

Equations (2.1) and (2.2) provide clear comprehension of the S parameters. Specifically, S_{11} is characterized as follows:

$$S_{11} = \frac{y_1}{x_1} | \; at \; x_2 = 0 \tag{2.3}$$

S_{11} indicates the amount of x_1 that is reflected back to y_1. S_{11} displays the input matching measurement for optimal power transfer. If the reflected power y_1 is 0, it indicates that all input power has been transferred. The S_{11} value is either 0 or $-\infty$ in logarithmic terms, indicating a perfect match. To achieve optimum power transfer, it is ideal for the practical value of S_{11} to be minimized, preferably below – 10 dB. The term S_{12} is defined as

$$S_{12} = \frac{y_1}{x_2} | \; at \; x_1 = 0 \tag{2.4}$$

The magnitude of S_{12} indicates the extent of power transfer from port_2 to port_1. It quantifies the effectiveness of isolation between port_1 and port_2, with a lower value signifying superior isolation from port_2 to port_1. The definition of S_{21} is as follows:

$$S_{21} = \frac{y_2}{x_1} | \; at \; x_2 = 0 \tag{2.5}$$

S_{21} represents the ratio of power at port_2 to power at port_1, elucidating the power gain of the two-port network. Likewise, the definition of S_{22} is as follows:

$$S_{22} = \frac{y_2}{x_2} | \; at \; x_1 = 0 \tag{2.6}$$

S_{22} evaluates the matching of the output port. Minimize the value of S_{22} to improve port_2 matching with the load and maximize power transfer to the load. An ideal amplifier should exhibit low values for S_{11}, S_{22}, and S_{12}, while having a high value for S_{21}. S_{11} is utilized for assessing input match, while S_{21} is employed for measuring LNAs power gain.

Analysis of the stability of the two-port network is conducted utilizing S parameters. The stability (K) requirement is defined by the S parameters as (2.7).

$$K = \frac{1 - |S_{22}|^2 - |S_{11}|^2 + |\Delta_s|^2}{2|S_{12}S_{21}|} > 1 \quad (2.7)$$

2.2 Performance Matrices of LNA

Key performance metrics of the LNA include:

- Gain of Power and Impedance Alignment
- Noise Figure (NF)
- Electrical Power Utilization
- Linearity (IIP3)
- Stability

2.2.1 Gain of Power and Impedance Alignment

The Low Noise Amplifier (LNA) is the initial amplification stage in a receiver designed to boost faint signals received from the antenna. To achieve maximum power transfer from the antenna's output to the LNA's input, the input impedance of the LNA must be matched to the output impedance of the antenna. When impedance is mismatched, signals are reflected back, causing noise. Input impedance matching is a crucial element in LNA design to optimize power transfer. S_{11} in the S-parameters of a two-port network represents the ratio of reflected signal power at port_1 to the input signal power. S_{11} is measured in decibels (dB) and a value below – 10 dB is the ideal target. A – 10 dB, S_{11} value indicates that 10% of the total input power is reflected back. For optimal transfer of amplified output power from the Low-Noise Amplifier (LNA) to the next stage input, the output impedance of the LNA should be matched with the input impedance of the next stage. The measurement of output impedance matching is determined by the S-parameter S_{22}. Another important design performance parameter is Power gain (S_{21}), which should be maximized to enhance the amplitude of weak received signals.

2.2.2 Noise Figure

The evaluation of the noise characteristics of a two-port network involves determining its Noise Factor (F). The Noise Factor represents the ratio of the total output noise power to the output noise originating from the input source. When expressed in dB, this Noise Factor is termed the Noise Figure (NF)

$$SNR = \frac{P_{signal}}{P_{noise}} \tag{2.8}$$

$$F = \frac{\frac{P_{s\_in}}{P_{n\_in}}}{\frac{P_{s\_out}}{P_{n\_out}}} \tag{2.9}$$

$$NF = 10\,log(F) \tag{2.10}$$

Where, SNR = Signal to Noise Ratio, P_{signal} = Signal power, P_{noise} = Noise power P_{s_in} = input signal power, P_{n_in} = the input noise power, P_{s_out} = output signal power and P_{n_out} = output noise power.

In electronic circuits, noise is a stochastic and non-deterministic variable. The presence of circuit noise is attributed to the characteristics of the materials utilized or external interferences. Noise causes signal degradation. It is necessary to thoroughly study and devise methods to limit the impact of noise on signals. The next section describes the primary sources of noise in the circuit [4], [5].

Thermal noise in circuits arises from the stochastic movement of electrons. The power (P) of the thermal noise signal is represented by equation (2.11).

$$P = KT\Delta f \tag{2.11}$$

Here, K denotes Boltzmann's constant, Δf is the system's bandwidth in Hz, and T represents the temperature in Kelvin. The model provided in equation (2.12) depicts the thermal noise voltage ($\overline{V_{th}^2}$) generated within a resistor.

$$\overline{V_{th}^2} = 4KRT\Delta f \tag{2.12}$$

MOSFETs also display thermal noise caused by the movement of carriers in the channel. The noise is represented by incorporating a current source in parallel with a MOSFET that has a conducting channel, as illustrated in Figure

2.2. This noise current ($\overline{I_n^2}$) is represented by equation (2.13) when the device operates in triode mode [6].

$$\overline{I_n^2} = 4KT\gamma g_{d0}\Delta f \tag{2.13}$$

In this context, γ represents the excess noise parameter, and g_{d0} is the drain-to-source conductance when V_{DS} equals 0. When a MOSFET is in saturation mode, the thermal noise current in the channel is modeled as illustrated in equation (2.14) [7].

$$\overline{I_n^2} = 4KT\gamma g_m\Delta f \tag{2.14}$$

Where, $\gamma = \frac{2}{3}$ [8] for long channel device, for short-channel and submicron MOSFETS, γ has higher values, in a range between 1 and 3 [9].

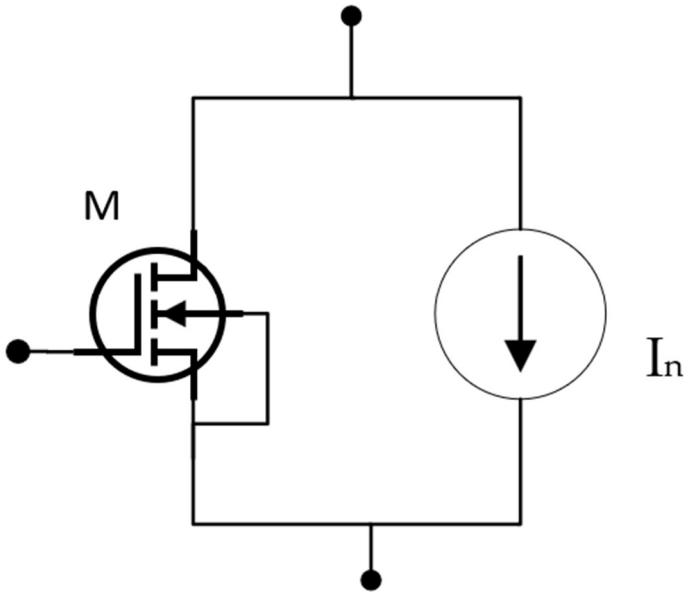

Figure 2.2: MOSFET channel thermal noise representation [7]

Thermal noise caused by dispersed gate resistance is another form of noise in MOSFETs. The gate resistance varies according to the MOSFET's geometry. Equation (2.15) represents the resistance of a single polysilicon gate finger (R_G) that is interconnected on both sides [10].

$$R_G = \frac{1}{12}\rho_{sh}\frac{W}{L} + \frac{\rho_{con}}{WL} \tag{2.15}$$

Where, ρ_{sh} is silicide sheet resistance, W and L is the width and length of the MOSFET channel and ρ_{con} is silicide to polysilicon contact resistance.

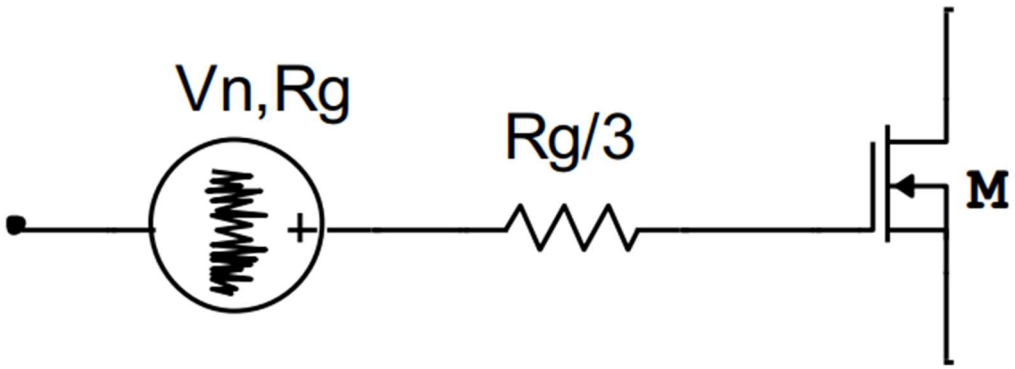

Figure 2.3: Equivalent noise model for gate resistance [5]

Figure 2.3 illustrates the equivalent noise model of a gate resistor, with $\frac{R_g}{3}$ representing the equivalent gate resistance and V_n, R_g representing the equivalent gate noise voltage [5], [11]. Enhancing silicide sheet resistance can be achieved through the use of a multi-finger gate design [10], [12], resulting in a reduction of gate resistance thermal noise. Should the power spectral density of the noise be notably lower than that of the channel thermal noise, it may be deemed inconsequential.

$$4KT\frac{R_G}{3} \ll \frac{4KT\gamma}{g_m} \tag{2.16}$$

The flicker noise in MOSFET is caused by a physical phenomenon and is characterized by its unpredictability. It encompasses the interaction between the silicon substrate (Si) and the gate oxide (SiO_2). Flicker noise emanates from the stochastic fluctuations in charge carriers within the channel, originating from the capture and emission processes of carriers at the silicon-silicon dioxide interface. Flicker noise decreases as frequency increases, making it insignificant at higher frequencies. Within the model, there exists a flicker noise voltage generator connected in series with the gate. The representation of this flicker noise ($\overline{V_{nf}^2}$) is articulated by equation (2.17).

$$\overline{V_{nf}^2} = \frac{Kf}{C_{ox}WLf} \tag{2.17}$$

Here, Kf denotes a process-dependent constant, while C_{ox}, W, and L represent the gate oxide capacitance per unit area, width, and length of the MOSFET, respectively. Notably, for p-channel devices, Kf exhibits a lower value compared to n-channel devices, leading to reduced flicker noise in PMOS transistors.

Shot noise arises from current fluctuations across a p-n junction potential barrier. Charge carriers diffuse randomly, resulting in varying speeds among carriers. The shot noise is defined as (2.18).

$$\overline{I_{ns}^2} = 2qI_{DC} \tag{2.18}$$

Shot noise results from the fluctuations in current around its mean value, with q representing the electron charge and I_{DC} denoting the direct current. Shot noise is more pronounced in bipolar junction transistors than in MOSFETs due to the fact that both emitter and collector currents contribute to the generation of shot noise. DC gate leakage current in MOSFETs generates shot noise but is often minimal and can often be disregarded.

2.2.3 Electrical Power Utilization

Efficient power management is an essential design consideration for products relying on battery power. A low power dissipation design not only extends battery life but also reduces cooling system costs and enables increasing chip complexity to integrate more functionality.

2.2.4 Linearity

In the design of LNAs, considering linearity is crucial, particularly when handling weak input signals and strong interference signals. Insufficient linearity in a system can led to cross modulation caused by powerful interference signals, resulting in unwanted intermodulation distortion.

The input-output relationship for a memoryless linear system is stated as equation (2.19).

$$y(t) = ax(t) \tag{2.19}$$

For a time-variant system, the function a is dependent on time, whereas for a time-invariant system, the function a remains constant. The input/output relationship of a memoryless nonlinear system is defined as equation (2.20) [13].

$$y(t) = a_0 + a_1x(t) + a_2x^2(t) + a_3x^3(t) + \ldots\ldots\ldots\ldots \quad (2.20)$$

The calculation of harmonics indicates that the gain experienced by $Acos(wt)$ is expressed as $\left(\alpha_1 + \frac{3\alpha_3 A^2}{4}\right)$, showcasing significant variations with increasing A. In instances where $\alpha_3 < 0$, resulting in a reduction in gain with an increase in A, this effect is quantifiable through the 1dB Gain compression point. This point denotes the input power level at which a signal induces a 1dB reduction in gain from its extrapolated value, as delineated in Figure 2.4. When presented on a logarithmic scale, the output power at a 1dB compression point deviates by 1dB from its ideal value relative to input power [13].

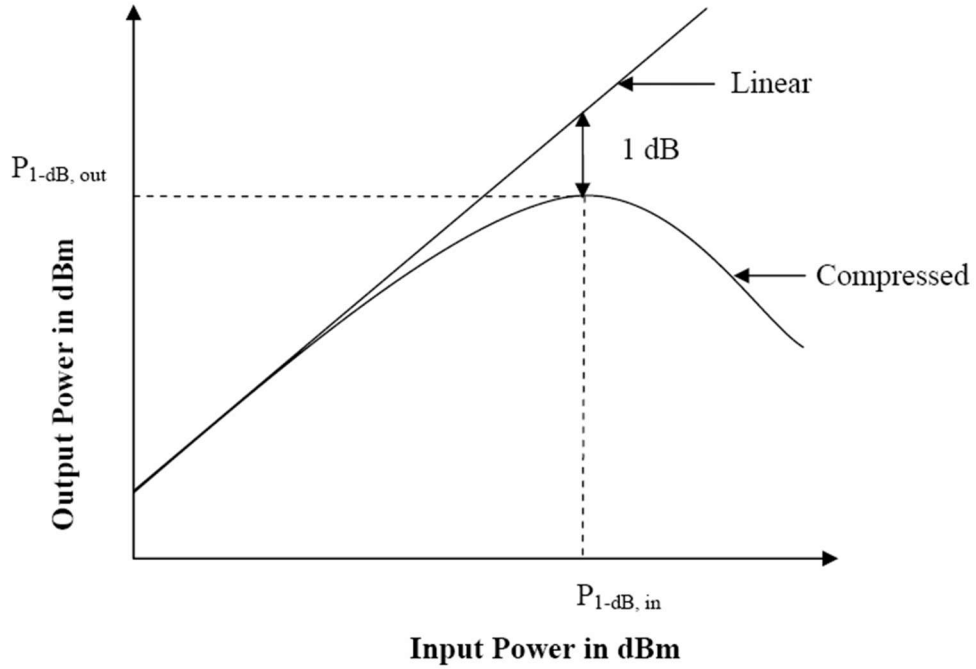

Figure 2.4: 1 dB compression point [13]

The computation of the 1 dB compression points entails establishing equivalence between the compressed gain and a value 1 dB lower than the ideal gain.

$$20\,log\left(\alpha_1 + \frac{3\alpha_3 A^2}{4}\right) = 20\,log(\alpha_1) - 1dB \tag{2.21}$$

A 1 dB compression signifies a 10% decrease in gain and is commonly employed to describe RF systems. Another negative consequence of compression arises when a powerful interfering signal is present alongside the received signal. In the time domain, the faint target signal is overlaid over the powerful interfering signal. As a result, the receiver's gain is diminished by the significant interference caused by the interferer, even if the desired signal is weak, a phenomenon known as "desensitization." This phenomenon diminishes the signal-to-noise ratio (SNR) at the output, a critical aspect even when the signal lacks amplitude information [13].

For a qualitative assessment of desensitization, consider $A_1\,cos(\omega_1 t)$ as the desired signal and $A_1\,cos(\omega_1 t)$ is desire signal and $A_2\,cos(\omega_2 t)$ as the interfering signal. The input to the amplifier is expressed as $x(t) = A_1\,cos(\omega_1 t) + A_2\,cos(\omega_2 t)$. The output of the nonlinear system manifests as –

$$y(t) = \left(\alpha_1 + \frac{3}{4}\alpha_3 A_1^2 + \frac{3}{2}\alpha_3 A_2^2\right) A_1\,cos\,\omega_1 t + \ldots\ldots\ldots \tag{2.22}$$

Therefore, the gain encountered by the desired signal is given by $\left(\alpha_1 + \frac{3}{2}\alpha_3 A_2^2\right)$, a diminishing function of A_2 when $\alpha_1\alpha_3 < 0$. An increase in the value of A_2 leads to a reduction in gain, eventually reaching zero. This circumstance is termed signal blocking. In RF design, the term "blocking signal" or "blocker" denotes interferers that desensitize a circuit, even without reducing the gain to zero [13].

2.2.5 Stability

The design of the MOSFET amplifier with high-power gain has been meticulously crafted to guarantee stability amidst changing input and output loading conditions. The stability factor K, derived from S parameters, is a

common metric used to analyze stability characteristics, as defined by equation (2.23).

$$K = \frac{1 + |\Delta|^2 - |S_{11}|^2 - |S_{22}|^2}{2|S_{21}||S_{12}|} \tag{2.23}$$

Where, $\Delta = S_{11}S_{22} - S_{21}S_{12}$, determinant of S parameter matrix. Value of K greater than unity and Δ less than unity make system unconditionally stable.

Amplifiers with high power gain (S_{21}) need the feedback parameter (S_{12}) to be minimal according to the expression for K. The cascode amplifier circuit enhances stability by decreasing the gain at the output of the driver transistor, resulting in a more unilateral device. The design of an LNA involves a multi-dimensional optimization issue. Trade-offs arise from the fact that optimizing individual specifications does not result in uniform sizing or biasing solutions. This underscores the necessity for designers to meticulously choose the optimal performance criteria tailored to the intended use of the LNA.

In conclusion, S parameters serve as indispensable tools for evaluating and refining the performance of RF circuits, notably LNAs, by enabling precise assessment of parameters such as impedance matching, power gain, and stability, thus facilitating the design of efficient and robust wireless communication systems.

3 Literature Review

This literature review chapter provides a comprehensive analysis of existing research pertaining to the design and performance analysis of CMOS amplifiers tailored for ultra-wideband wireless receivers, with a specific focus on the integration of Substrate Integrated Waveguide (SIW) resonators. It aims to examine the current state of knowledge in this field, identify key research trends, and establish a foundation for the subsequent investigation presented in this thesis.

3.1 Wideband LNA Implementation Approaches

Three alternative ways can be used to implement a multi-standard LNA. Utilizing separate narrowband LNAs for each communication standard is a straightforward method that is easy to construct and delivers exceptional results. However, the power consumption and silicon space needed for several LNAs might be significant. Using a multiband/band switching LNA. Multiband technology is more power-efficient than narrow band LNAs but necessitates a greater area due to the utilization of bigger tuning inductors [14] – [19]. The third way utilizes a single wideband LNA to process all standards simultaneously. The broadband LNA is more cost-effective and space-efficient than the first and second techniques, but it has a downside of having a modest power gain [20] – [27]. A broadband LNA may effectively support many standards [28]. Wideband LNAs provide consistent gain, input impedance matching, noise figure (NF), and third-order input intercept point (IIP3) across their whole frequency range.

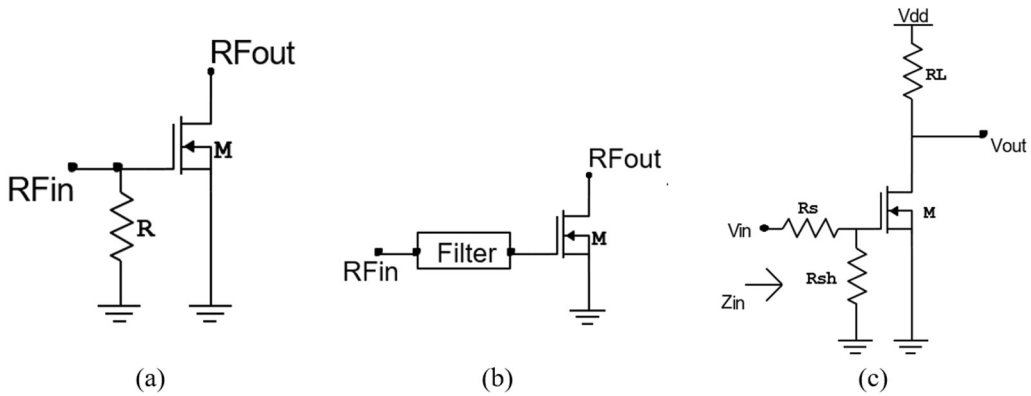

Figure 3.1: (a) Resistive termination, (b) Common gate, (c) Feedback LNA topology [14]

Various topologies utilized in literature for wideband input matching include resistive termination common source, common gate, feedback, CS with wideband input filter, and distributed, as seen in Fig. 3.1 and Fig. 3.2.

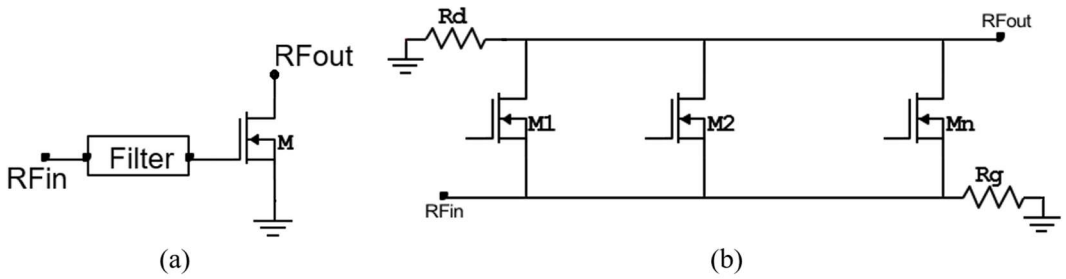

Figure 3.2: (a) Filter, (b) Distributed LNA topology [15]

3.2 Common Source with Resistive Termination LNA Topology

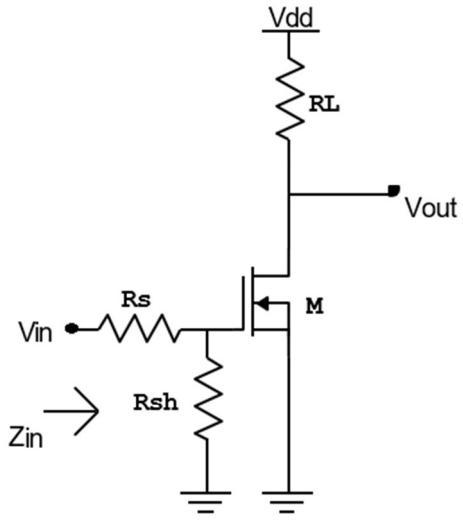

Figure 3.3: Common Source (CS) with resistive termination topology [16]

To achieve wideband input impedance matching, one way is to add a shunt resistor at the input of the CS LNA, as seen in Figure 3.3.

Voltage gain of resistive termination is expressed as

$$A = -g_m R_L \left(\frac{R_{sh}}{R_s + R_{sh}}\right) \tag{3.1}$$

Where, R_{sh} = shunt resistance, R_s = series resistance and R_L = load resistance. For $R_{sh} = R_s$ voltage gain is simplified as –

$$A = -g_m \left(\frac{R_L}{2}\right) \tag{3.2}$$

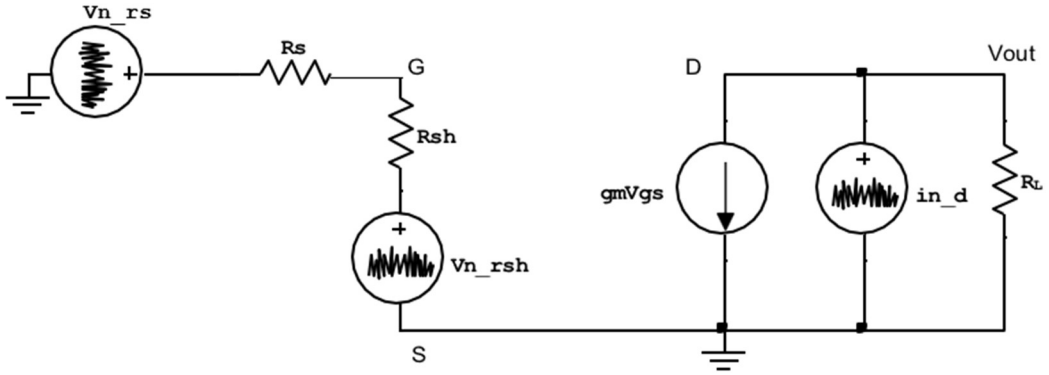

Figure 3.4: AC equivalent circuit with noise sources of resistive termination CS

The resistive termination gain at input matching is half of the Common source gain ($-g_m R_L$) as demonstrated in equation (3.2). Noise figure is a measure of the degradation of the signal-to-noise ratio by a device or system.

$$F = \frac{Total\ output\ noise\ power}{Output\ noise\ due\ to\ input\ source} \tag{3.2}$$

Total noise figure of this topology can be expressed as

$$NF = 2 + \frac{4\Upsilon}{g_m R_s} \tag{3.3}$$

Where, Υ is a noise parameter and $R_{sh} = R_s$ is shunt resistor value. Limitations of this topology are:

- ✓ Poor noise figure
- ✓ Input signal is dampened by a voltage divider, resulting in a reduction of gain.
- ✓ R_{sh} adds extra thermal noise.
- ✓ To accommodate the additional shunt inductor at higher frequencies, it is necessary to adjust the input capacitance C_{gs}.

3.3 Common Gate Topology

The Common Gate (CG) amplifier inherently presents extensive input matching capabilities. Equation (3.4) denotes the expression for the input impedance of the common gate configuration.

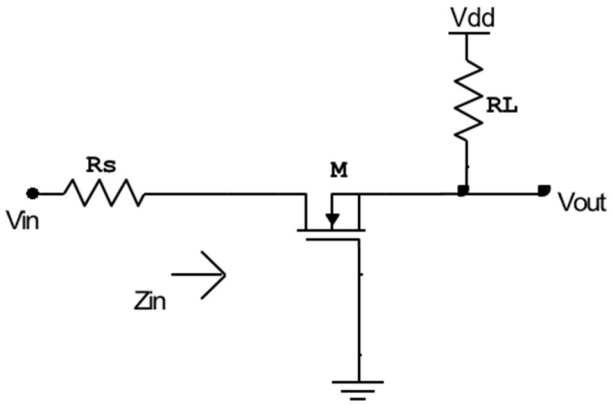

Figure 3.5: Common Gate (CG) topology [17]

$$Z_{in} = \frac{1}{g_m} \tag{3.4}$$

Where, Z_{in} is the input impedance and g_m is transconductance of the MOSFET

3.3.1 Analysis Noise Figure of CG

The Common Gate (CG) topology encounters noise originating from two distinct sources: the source resistor and MOSFET channel noise. The Noise Figure (NF) of the Common Gate (CG) is formally represented by equation (3.5), when input impedance match $R_s = \frac{1}{g_m}$.

$$NF = 1 + \Upsilon + \frac{4R_s}{R_L} \tag{3.5}$$

The Noise Figure (NF) of a Common-Gate (CG) topology can be calculated using equation (3.5), where Υ is the process-dependent noise parameter. Increasing the transconductance (g_m) of a common gate (CG) configuration improves its Noise Figure but reduces its wideband input matching. The tradeoff involves setting the (g_m) value to achieve both low noise figure and wideband matching. To decrease the impact of Miller capacitance in a common gate (CG) configuration, one can utilize a cascode structure with a common source (CS).

The input impedance of a common gate with common source cascode structure is represented by equation (3.6).

$$Z_{in} = \frac{1}{g_m + g_{mb}} \tag{3.6}$$

Where g_m and g_{mb} represent the transconductance of the transistors. The main disadvantages of the CG architecture include poor gain, increased Noise Figure (NF) with wideband matching, and high-power consumption [29], [30].

Various hybrid topologies with conjugate matching were employed in literature to achieve broad frequency coverage, low noise figure, and high-power amplification [14, 17, 31]. Positive feedback in the common gate configuration relaxes the constraint on selecting transconductance (g_m) for input matching. Positive feed-back increases loop gains and decreases overdrive voltage, leading

to a degradation in linearity and noise figure performance [32]. The feedback circuit intentionally utilizes an inverted amplifier to improve transconductance. Negative feedback in the control group decreases noise figure and power usage, but it has compromised the stability of the design. The positive-negative feedback gain-boosted design technique provides enhanced noise figure and amplification without compromising linearity and input impedance matching. It has yielded equivalent power enhancement to positive feedback while utilizing only half the electricity. Different methods including dual negative feedback and noise cancellation are employed with common gate to enhance the performance of the Low-Noise Amplifier.

The paper [33] utilized parallel common source with CG to balance the tradeoff between input impedance matching and noise figure of the CG amplifier. Various distortion cancellation approaches are utilized with the CG to enhance linearity [21, 34, 35, 26].

3.4 Feedback LNA Topologies

Utilizing negative feedback in low-noise amplifiers is a common method to provide broad input impedance matching while maintaining low noise figure. Several unfavorable feedback LNA configurations are displayed in Figure 3.6. Using a lossless transformer as feedback provides optimal performance but necessitates a bigger silicon area [36]. Resistors in the feedback network, such as series RC, parallel RC, and transistors, are frequently employed. The utilization of negative feedback architecture contributes to the improvement of the noise figure and input impedance matching of the device.

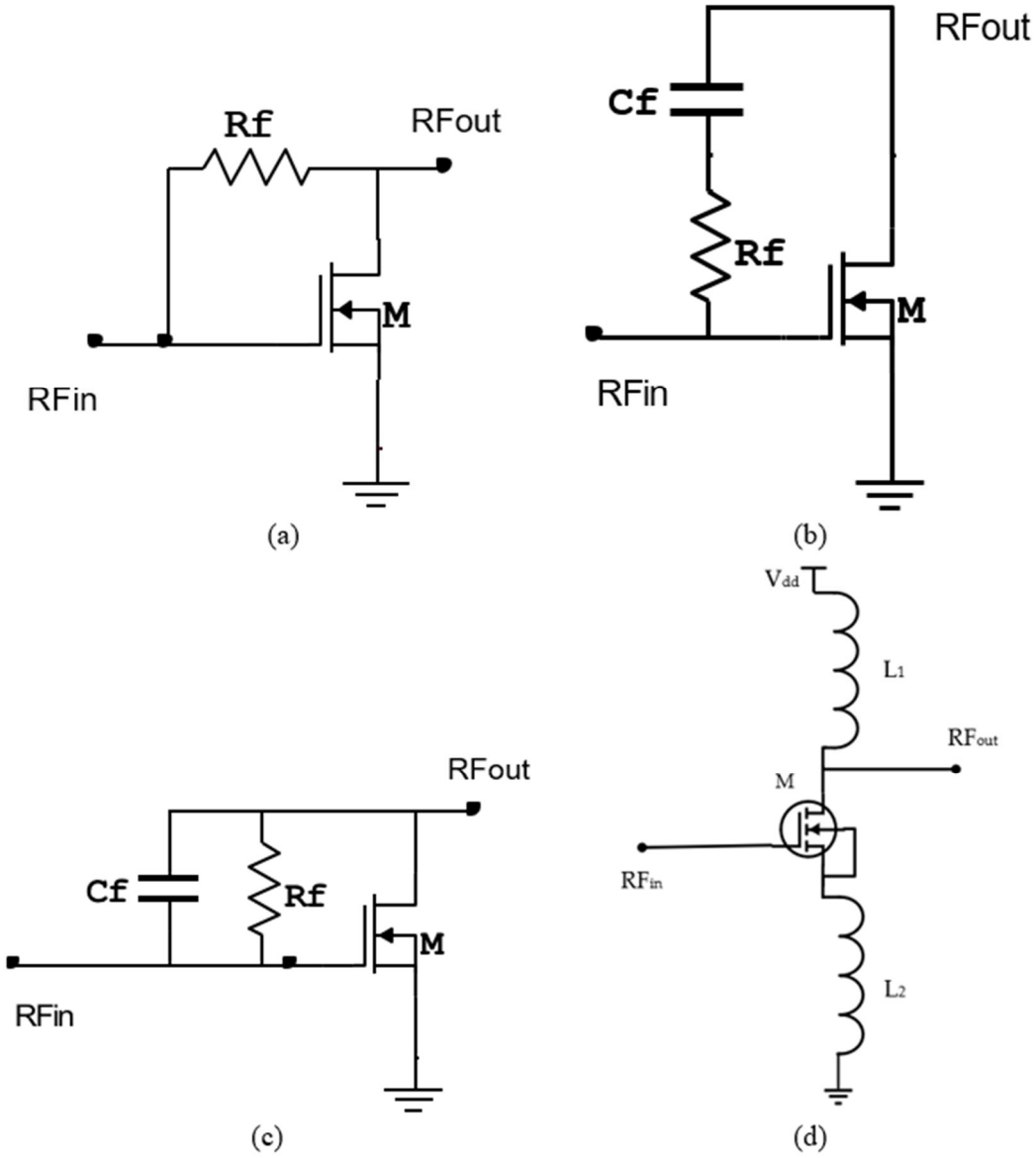

Figure 3.6: Feedback topologies a) resistive b) series RC c) parallel RC and d) transformer

3.4.1 Resistive Feedback LNA Topology

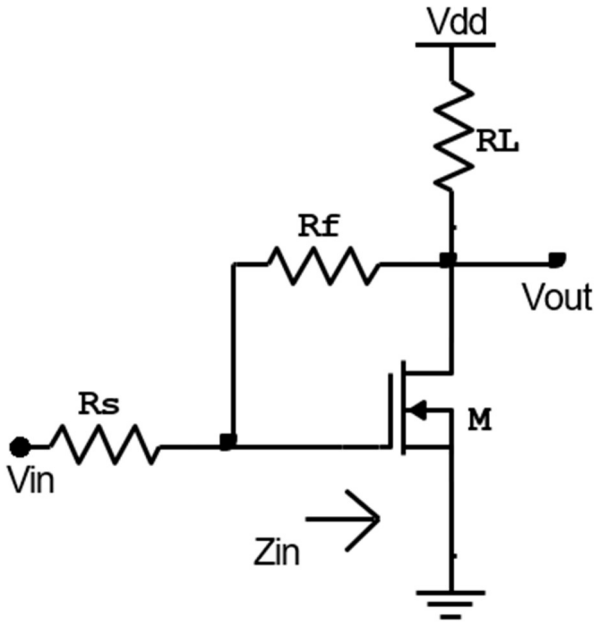

Figure 3.7: Resistive feedback common source (CS) topology

3.4.1.1 Gain Analysis

Resistive feedback amplification the topology of a CS can be determined from its AC equivalent circuit, illustrated in figure 3.8.

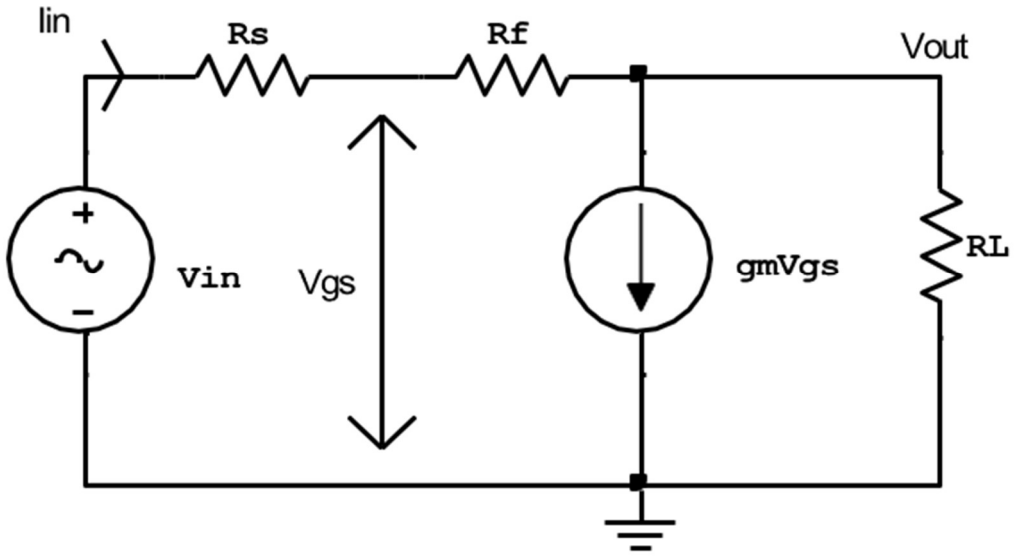

Figure 3.8: AC equivalent circuit of resistive feedback CS topology

Using Kirchhoff's Current Law in the input loop results in the relationship between input and output voltages.

$$V_{in} = i_{in}(R_s + R_f) + V_{out} \tag{3.7}$$

$$V_{out} = (i_{in} - g_m V_{gs})R_L \tag{3.8}$$

$$V_{gs} = (i_{in}R_f + V_{out}) \tag{3.9}$$

Where, R_s, R_f and R_L are source, feedback, and load resistor, respectively. If $R_f \gg R_c$ & $g_m R_f \gg 1$ then gain equation can be simplify as

$$A_{V,tot} = \frac{-g_m R_L}{R_s + R_f + R_L + g_m R_s R_L} \cong -g_m R_L \tag{3.10}$$

The input impedance of a resistive feedback common source amplifier is represented by equation (3.11).

$$Z_{in} = \frac{R_f + R_L}{1 + g_m R_L} \tag{3.11}$$

3.4.1.2 Noise Figure Analysis

A resistive feedback amplifier experiences noise from three sources: source resistor, feedback resistor, and MOSFET. Total noise is the cumulative sum of all separate source noises.

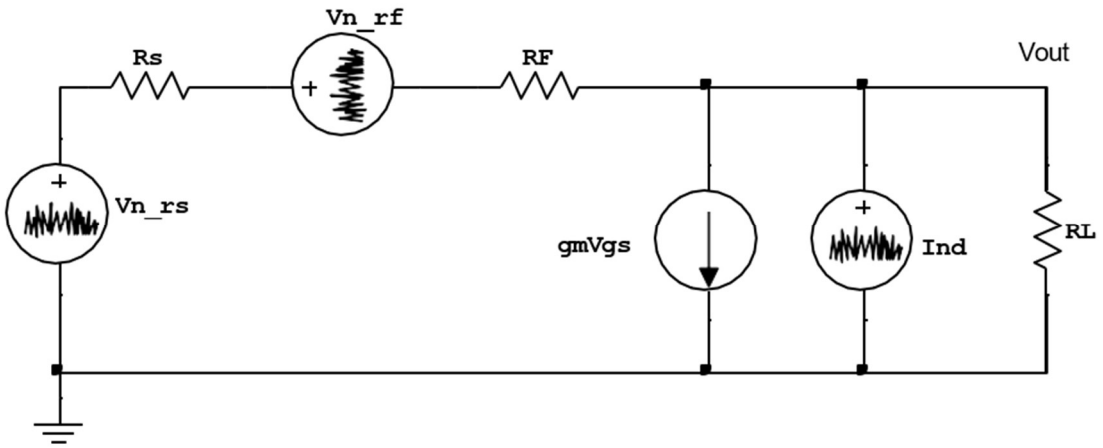

Figure 3.9: AC equivalent circuit with noise sources of resistive feedback CS [37]

To determine the output noise caused by the feedback resistor, isolate the feedback resistance noise source and set all other sources in Figure 3.9 to zero.

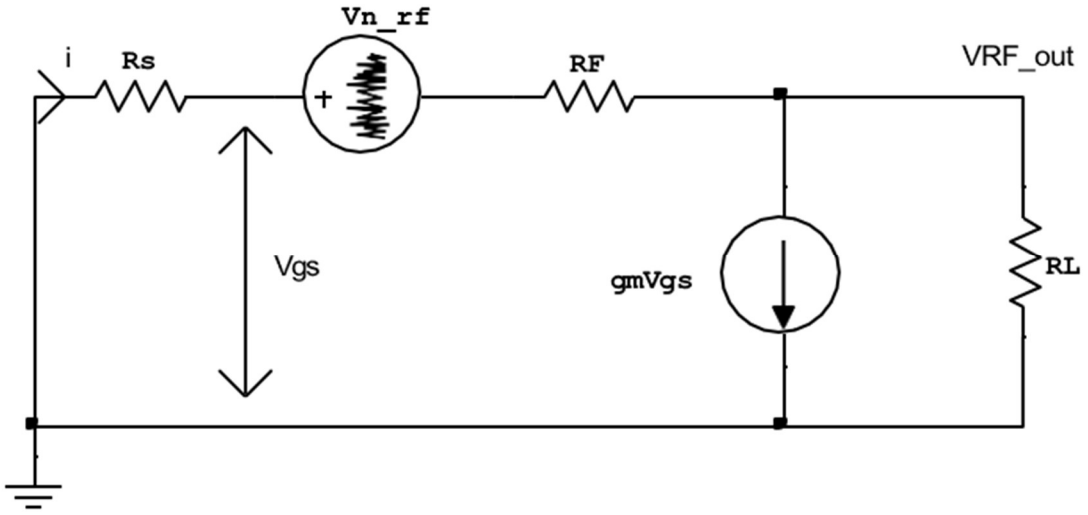

Figure 3.10: Feedback resistance noise of resistive feedback CS [38]

Total noise figure is.

$$NF = 1 + \frac{\overline{V_{n,RF}}^2 \left[\frac{R_L}{R_f}(1 + g_m R_s)\right]^2}{A_V{}^2 \overline{V_{n,Rs}}^2} + \frac{\overline{I_{nd}}^2 R_L{}^2}{\overline{V_{n,Rs}}^2 A_V{}^2} \tag{3.12}$$

$$NF = 1 + \frac{R_S}{R_f}\left(1 + \frac{1}{g_m R_s}\right)^2 + \frac{\Upsilon}{g_m R_s} \tag{3.13}$$

Equation (3.13) demonstrates that the noise figure of resistive feedback is inversely proportional to R_f and $g_m R_s$. Increasing the feedback resistance value NF improves the design but worsens input impedance matching. A trade-off exists between noise figure and input matching in resistive feedback topology. A gate inductor is required in a resistive feedback CS amplifier at higher frequencies to eliminate the effect of C_{gs} and enhance gain.

Increasing the amount of the feedback resistor improves noise figure but negatively impacts linearity, input matching, and flat gain performance. The current inverter structure utilizes resistive feedback with NMOS/PMOS pair to enhance linearity, as discussed in references [37], [38]. This topology has a limitation of low bandwidth and utilizes an additional transistor for feed-forward noise suppression, leading to increased power dissipation. Resistive feedback topologies in references [25], [39], [40] are utilized to produce improved

wideband performance using noise and distortion cancellation methods. The studies utilized resistive feedback with NMOS/PMOS pair in a cross-coupled manner for noise cancellation as referenced in [41], [42]. The design attained a remarkably low noise figure of 1.43 dB. To enhance noise figure in the design, large-size transistors were utilized, leading to a degradation in high-frequency response caused by the rise in parasitic capacitance.

Parasitic capacitance in resistive feedback circuits impairs the higher frequency response. Reactive feedback in literature enhances higher frequency response but necessitates a larger silicon surface.

3.4.2 Reactive Feedback LNA Topology

Reactive feedback can be achieved by using a series RC, parallel RC, or series RLC circuit as a feedback network. The LNA [43] utilized series RC feedback with series and shunt inductive peaking to enhance bandwidth, noise figure, and gain flatness. However, this device lacks linearity.

The systems [44] – [48] utilize parallel RC feedback, depicted in Fig. 3.6 (c), to provide broadband operation (3.1–10.6 GHz) and enhanced noise figure. However, these devices also exhibit poor linearity.

The architecture [49] utilized series RLC feedback for wideband operation spanning from 3.1 to 10.6 GHz. This system utilizes positive and negative feedback to achieve low noise figure and enhance input matching, albeit at the expense of increased power consumption.

Figure 3.6 (d) illustrates the transformer feedback Low-Noise Amplifier (LNA) topology [50] – [52]. The LNA [52] utilized transformer feedback and current reuse to attain low noise figure and low power usage. This design has a drawback of needing a bigger silicon area and exhibiting poor linearity.

3.4.3 Active Feedback LNA

The active feedback circuit consists of a common source amplifier in the input stage and a common drain amplifier in the feedback stage [53]. The

transconductance of the common drain stage determines the input impedance, whereas the transconductance of the common source amplifier affects the gain and noise figure of the entire Low-Noise Amplifier (LNA). Active feedback provides an additional level of control to adjust input impedance and noise figure apart from the design. The primary drawback of this architecture is the increased power consumption caused by the addition of the feedback step.

3.5 Distributed Amplifier LNA Topology

Distributed amplifiers are commonly utilized in the construction of wideband low-noise amplifiers [54]. The many phases of a typical common-source distributed amplifier design use increased power and necessitate a bigger silicon footprint. Wideband frequency response is attained by creating transmission lines by the combination of the parasitic capacitances of transistors with inductors. Distribution amplifiers often have consistent amplification, strong linearity, and naturally low noise figure [29], [20], [55].

Power consumption in data acquisition can be decreased by employing current reuse techniques or reducing voltage. [56] describes a low-power LNA (90 nm CMOS) designed with two distributed amplifiers arranged in a matrix configuration employing tapered transmission lines. This design exhibits substantial inversion bias to decrease power dissipation to 12.5 mW and attain a bandwidth of 21 GHz, a gain of 15.4 dB, but at the expense of poor linearity ($IIP3 = -6\ dBm$).

Various strategies for improving neural network performance are utilized in deep architectures. DA substitutes resistive termination with series RL circuit to decrease thermal noise caused by the terminating resistor. This approach necessitates two power supplies, resulting in increased power consumption and subpar input impedance matching.

DA technology is not ideal for portable and compact device receivers because it has significant power consumption and necessitates a bigger silicon

area. DA is commonly utilized in instrumentation and medical imaging applications.

Zhang and colleagues developed a wideband Low-Noise Amplifier (LNA) utilizing DA architecture to decrease power consumption by 9 mW through biasing transistors in moderate inversion [57].

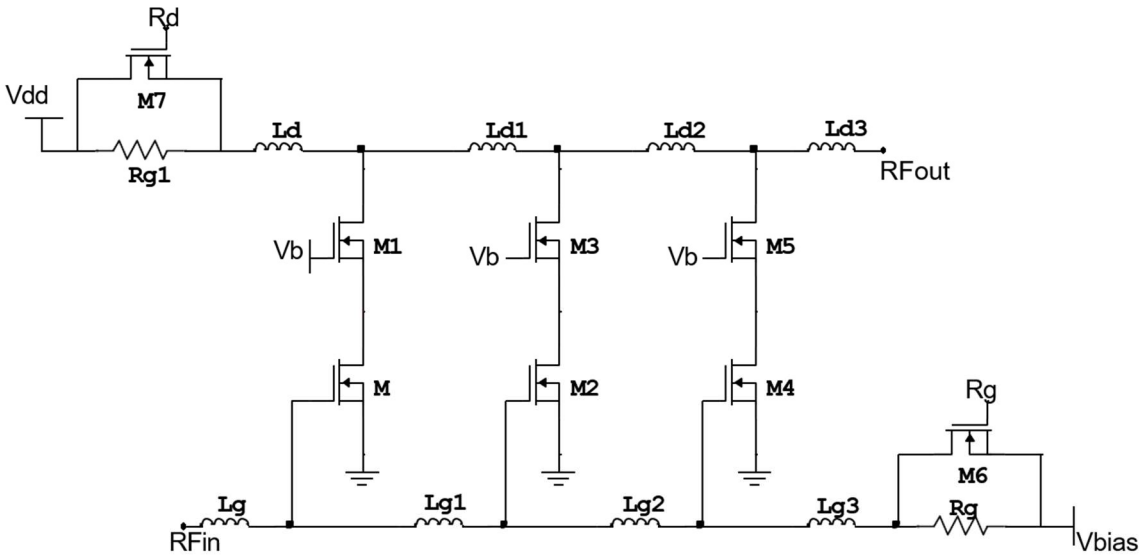

Figure 3.11: Cascode DA Schematic [57]

The mm-wave circuit has garnered significant interest due to developments in CMOS technology [58]. The low noise amplifier (LNA) is an essential component in a wireless network that requires high gain to minimize noise from following circuits and improve the system's sensitivity [59]. Yet, designing LNAs at mm-wave frequencies has hurdles in achieving high gain and low power consumption. Passive neutralization has been a popular and effective method for achieving high gain. Nevertheless, it is not advisable to fully utilize the active gadgets. To maximize the benefit, utilize a feedback circuit [60]. A T-shaped inductor can serve as an effective feedback circuit option because of its higher inductance characteristics [61].

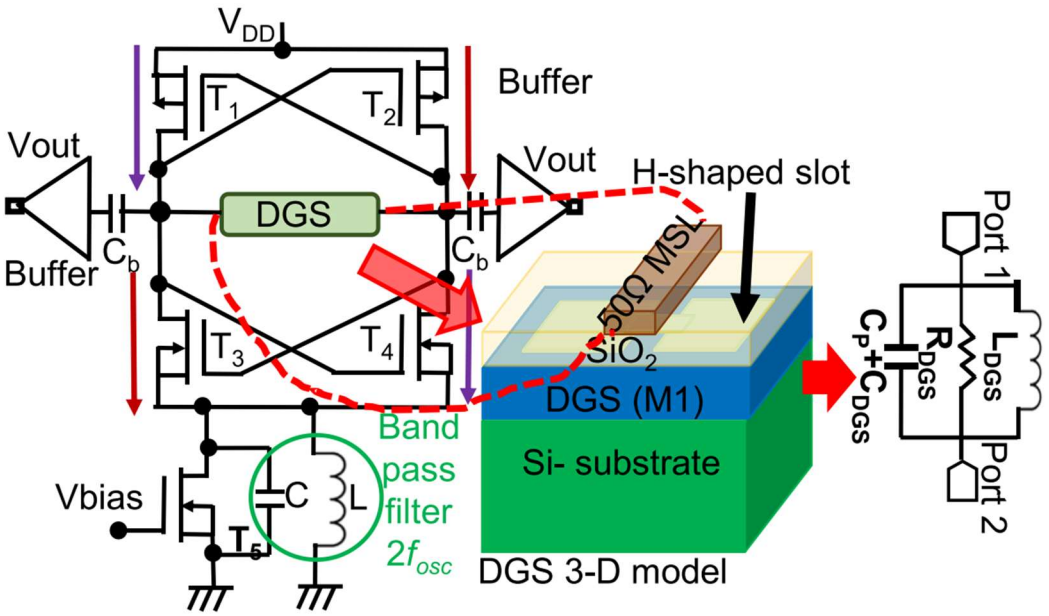

Figure 3.12: Cross-coupled oscillator with DGS resonator [62]

Figure 3.12 displays a voltage-controlled oscillator with a Defected Ground Structure (DGS) resonator. Conventional spiral inductors in the CMOS front end circuits block exhibit low self-resonant frequency, reduced quality factor, and high die area. To address these issues, researchers suggested an inductor-less block using virtual inductors created using a defective ground structure [62] – [66].

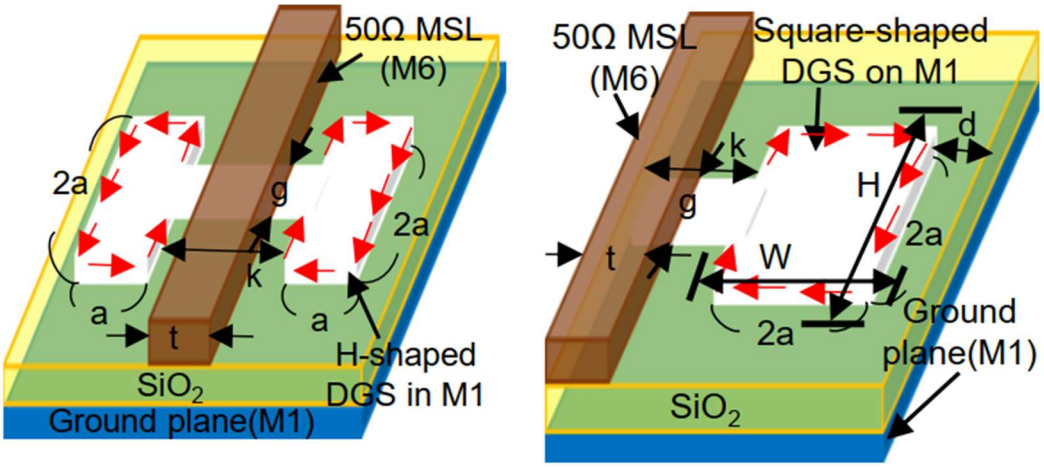

Figure 3.13: H – shaped and Square – shaped DGS resonator [63]

They provided actual evidence of the idea of illuminating an active inductor by employing a virtual inductor. The work was improved by producing a high Q-factor and increasing self-resonance within the Defected Ground Structure (DGS) in the addition of extra resonant characteristics [67], [68]. The characteristics of DGS at millimeter wave frequency are still unknown and have not been investigated.

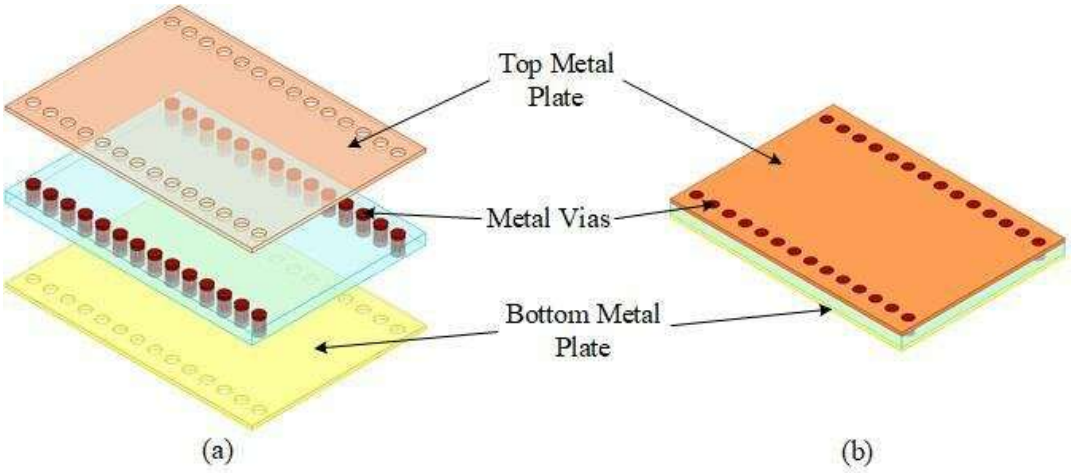

Figure 3.14: SIW 3D Model (a) Exploded View, (b) Normal View [69]

An innovative technique known as substrate-integrated waveguide (SIW) has been unveiled. SIW resonators have attracted considerable interest recently due to their inherent benefits, such as high-quality factor (Q-factor), compact size, and suitability for integrated circuit technology. SIW is superior to conventional rectangular waveguides because of its cost-effectiveness, little signal attenuation, good quality, high power-handling capabilities, ease of manufacture, compact size, and easily integrated components. SIW was once utilized for filter, antenna, and several other planar circuits [69] – [71]. Research on the SIW properties in CMOS technology is currently in progress. SIW is utilized in CMOS LNA for the first time as a replacement for a complementary active inductor.

Table 3.1: Summary of detail literature survey of the wideband LNA

Source	CMOS Technology (μm)	BW (GHz)	S_{21} (dB)	S_{11} (dB)	S_{22} (dB)	NF (dB)	Topology
[72]	0.18	3.1 – 10.6	9.5	< - 8.6		3 – 5.6	Cascode with input filter and current reuse
[33]	0.18	3.1 – 10.6	9.7	< - 11		4.7	CG with noise cancellation
[46]	0.18	3.1 – 10.6	13.9	< - 9.4		4.7	Parallel RC FB
[73]	0.18	3.1 – 10.6	13	- 8.6		4.68	CS + RLC input filter
[74]	0.18	2.4 – 11.2	14.8			3.9	CG + current reuse
[75]	0.18	3.1 – 10.6	15	< - 11		3.5 – 3.9	Inverter with FB
[76]	0.18	2.5 – 16	11	< - 7		3.3	RC FB CS + current reuse
[77]	0.13	3.5 – 5	14	< - 15		3.5 – 3.9	Fully differential + active FB + Noise cancellation
[78]	0.09	4	20.2	< - 11	< - 16	8.8	1 CS + 2 Cascode + inductor
[79]	0.065	10	21.5	< - 8	< - 9	6.7	4 stage cascode + inductor
[62]	0.18	1	17.2	< - 15	< -12	2.85	1 stage + H-shaped DGS
[63]	0.18	1	12.68	< - 13.5	< - 10	3.14	2 stages + square -shaped DGS
[80]	0.18	2.4 – 13	15.02	< -9.4	< - 15.8	4.4	FB resistor + LG inductor + inductive divider

Source	CMOS Technology (μm)	BW (GHz)	S_{21} (dB)	S_{11} (dB)	S_{22} (dB)	NF (dB)	Topology
[81]	0.18	6	19.79	< - 12.2	< - 13	2.03	Cascode inductive source degeneration
[82]	0.18	0.1 – 6	12.5 – 15.5	< - 10		3 – 4.5	Balun LNA
[83]	0.18	0.05 – 5	22.5 – 25.3	< - 10		3.6 – 5	Balun LNA
[84]	0.18	3.1 – 10.6	10.25 – 12.5	< - 11		3.5	Current Reuse
[85]	0.09	3 – 14	15.9 – 16.5	< - 10.2		5.68	Self-Body Biased Common Gate
[86]	0.09	1 – 13.18	15	< - 12.2		3.9	Current Reuse

4 UWB LNA Design and Optimization

This chapter delves into the methodology and design process behind developing and optimizing Ultra-Wideband (UWB) Low Noise Amplifiers (LNAs), particularly focusing on the integration of Substrate Integrated Waveguide (SIW) technology. It outlines the systematic approach taken to construct the LNA design and prepares the groundwork for assessing its performance against existing literature.

4.1 Design of SIW Resonator

SIW is a structure that transmits signals using a guided wave between top and bottom parallel metal layers. Metallic vias are utilized to establish connections between the upper and lower metal layers. A substrate is positioned amidst two parallel metal plates. Figure 4.1 displays the top view and cross section of the resonator. Figure 4.2 shows the bottom view of metal1 of the resonator. The SIW structure is created by selecting suitably spaced vias (P_h) of same dimension (D_m) to effectively sustain guided wave propagation while minimizing radiation loss. The effective width of substrate integrated waveguide (SIW) can be calculated using equations (4.1), (4.2), and (4.3) [87].

$$W_S = W - 1.08\frac{D_m^2}{P_h} + 0.1\frac{D_m^2}{W} \tag{4.1}$$

$$W_S' = \frac{W_S}{2} \tag{4.2}$$

The optimal via diameter and pitch to minimize radiation loss due to field leakage between vias can be calculated using equations (4.3), (4.4), and equation (4.5) [88], [89].

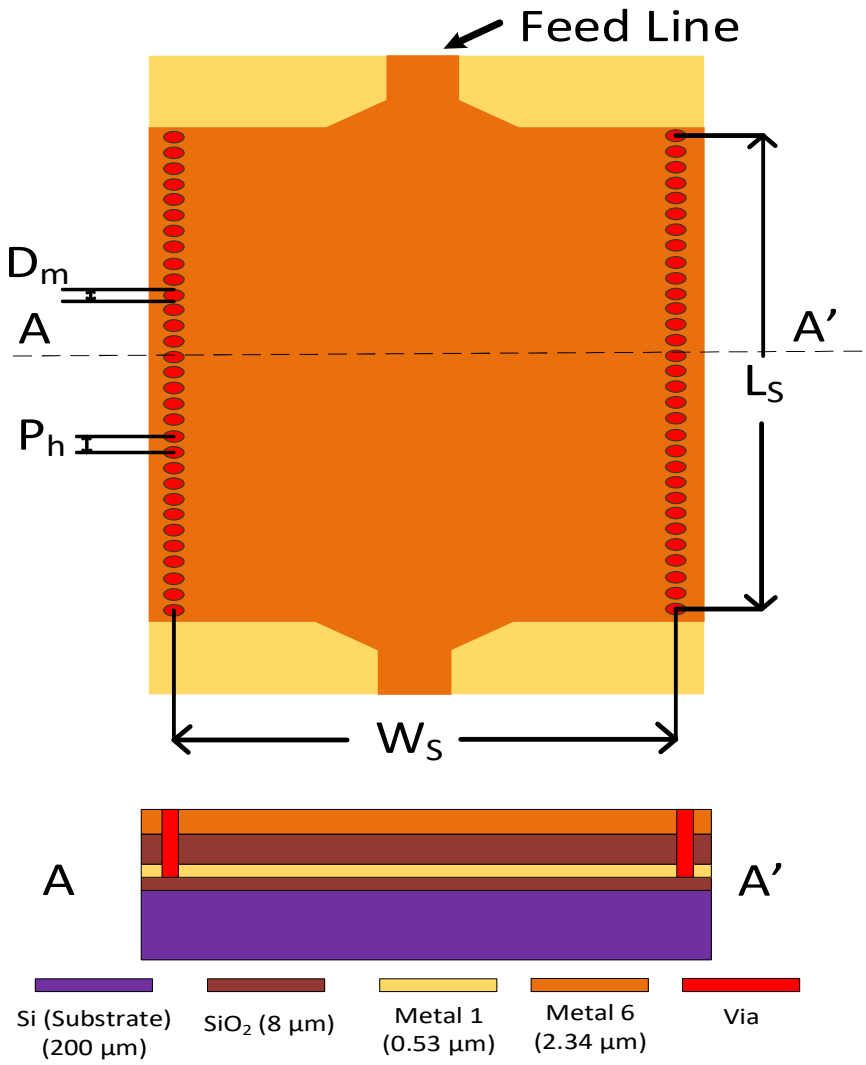

Figure 4.1: Cross section and schematic diagram of the proposed SIWs

$$P_h \leq 2D_m \tag{4.3}$$

$$D_m < 0.2\lambda_g \tag{4.4}$$

$$\lambda_g = \frac{c}{f\sqrt{\varepsilon_r}} \tag{4.5}$$

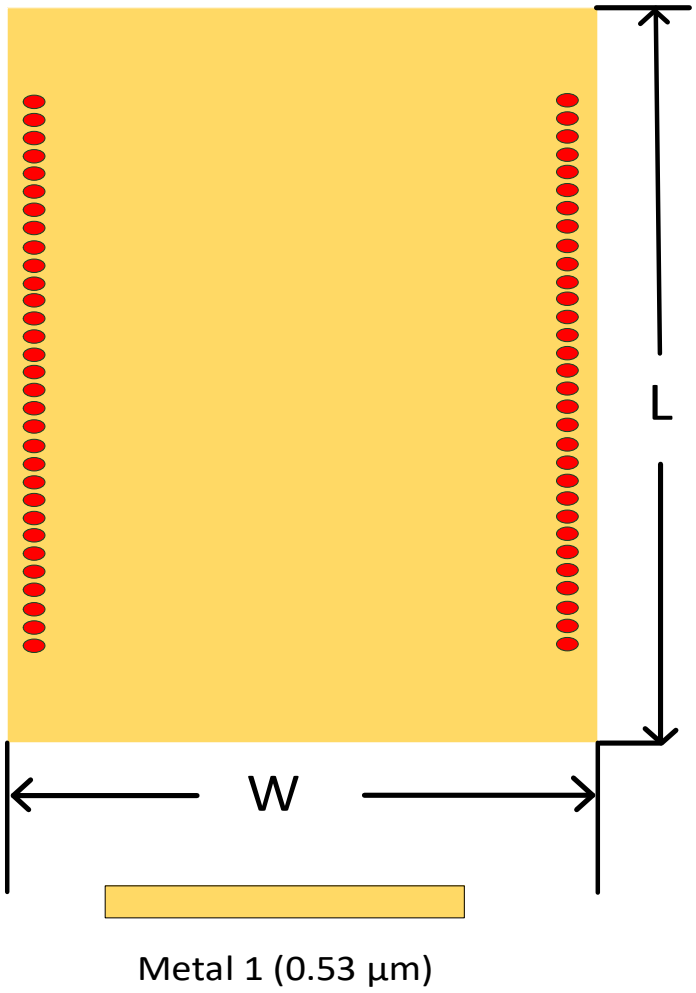

Figure 4.2: Bottom view the SIWs from metal1

Here, a represents the width of the substrate integrated waveguide (SIW), D_m is the diameter of the vias, P_h is the spacing between two adjacent vias, λ_g is the guided wavelength, c is the velocity of light in a vacuum, and f_r is the design frequency. Equation (4.6) can be used to determine the resonant frequency of the Substrate Integrated Waveguide (SIW) structure.

$$f_r = \frac{C}{2\sqrt{\varepsilon_r}}\sqrt{\left(\frac{1}{W_S}\right)^2 + \left(\frac{1}{L_S}\right)^2} \tag{4.6}$$

Where, W_S effective width of SIW, and L_S effective length of SIW. The Q factor can be characterized by employing the subsequent relationships [87].

$$Q = \frac{Img\ [Z]}{Real\ [Z]} = \frac{\omega L}{R_s} \tag{4.7}$$

Here, Z = input impedance.

4.1.1 Performance of the proposed SIW

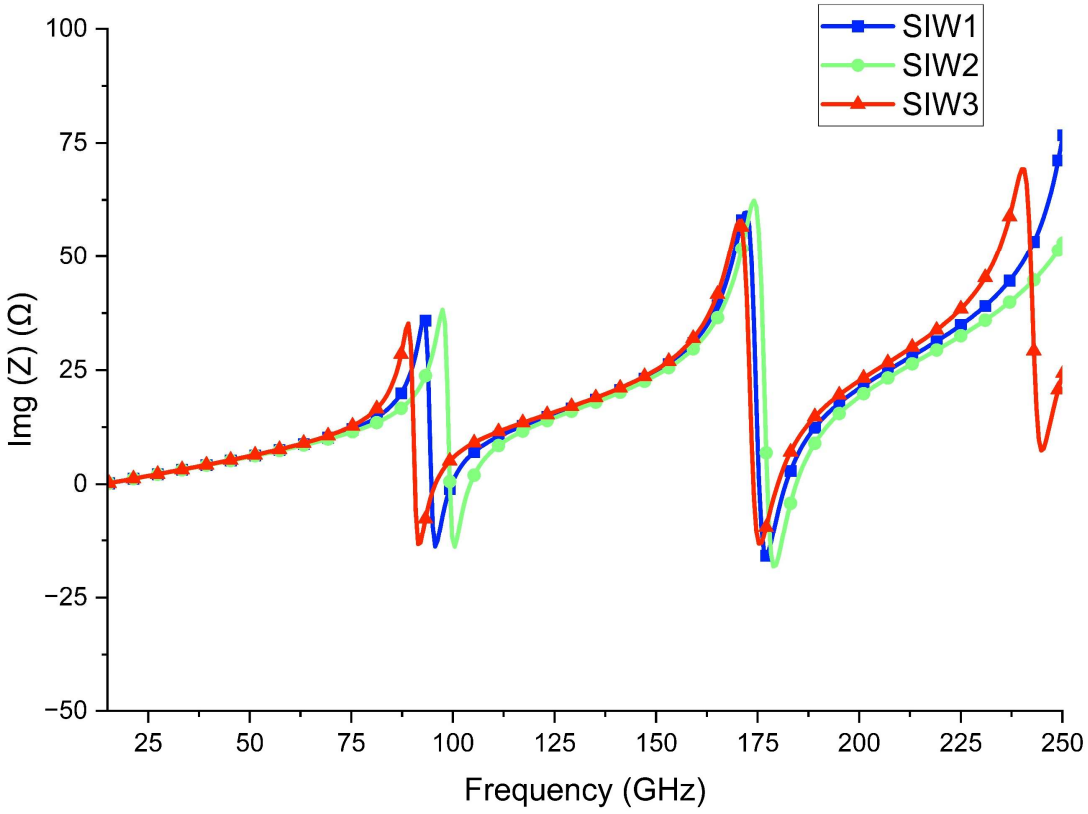

Figure 4.3: $Img(Z)$ of the designed SIWs

SIW acts as a resonator, offering inductive and capacitive values. Figure 4.3 displays the performance of its imaginary part of impedance ($Img(Z)$). The required bandwidth is 67.5 to 71.5 GHz. We developed the Substrate Integrated Waveguides (SIWs) to resonate at frequencies exceeding 90 GHz to improve performance in this bandwidth, even though it surpasses our intended Low-Noise Amplifier (LNA) working frequency. We aimed to design a low noise amplifier with a consistent inductance value at a specific operating frequency. We modified the substrate integrated waveguide (SIW) settings to get a flatter response in the imaginary part of the impedance ($Img(Z)$) response, while also increasing the Q value. The optimal parameters for Substrate Integrated Waveguides (SIWs) are presented in Table 4.1.

Table 4.1: Parameters of Designed SIWs

Design	We (μm)	L (μm)	D_m (μm)	P_h (μm)	f_r (GHz)	L_S (μm)	W_S (μm)
SIW1	650	700	10	16	90	590	620
SIW2	550	700	10	16	90	590	520
SIW3	800	700	10	16	90	590	770

We have created three Substrate Integrated Waveguides (SIWs) for use in our proposed Low Noise Amplifier (LNA). Figure 4.4 shows that the imaginary part of the impedance of the planned substrate integrated waveguides is flat. Which states that the inductance value remains constant at higher frequencies. At higher frequencies, a spiral inductor behaves resistively. SIW can be substituted with an inductor to enhance performance.

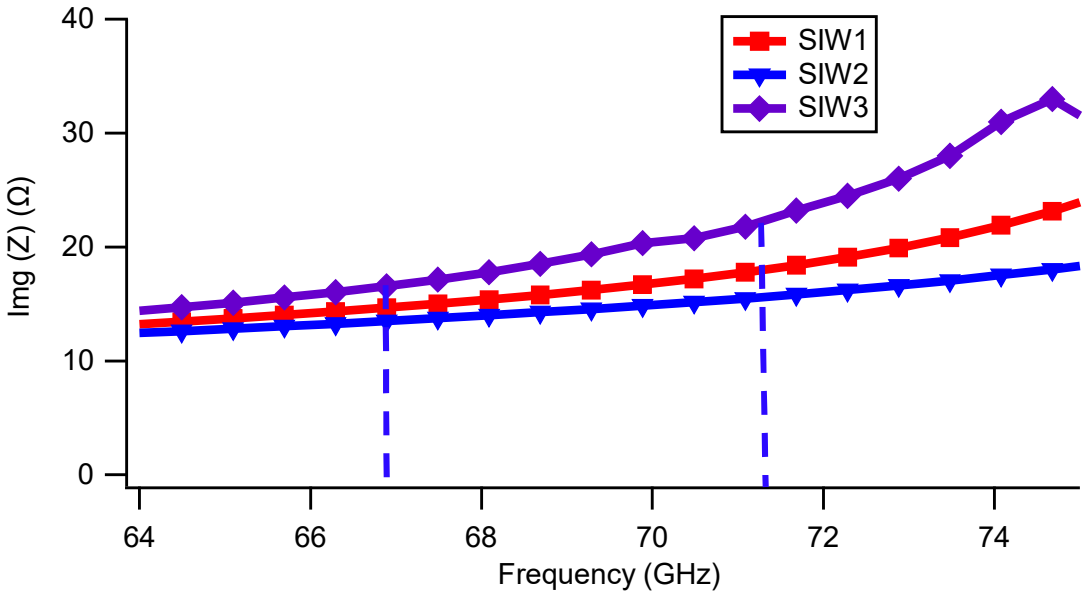

Figure 4.4: $Img(Z)$ of the designed SIWs for required bandwidth

Satisfactory values are required for both the imaginary part of the impedance ($Img(Z)$) and the quality factor (Q). Figure 4.5 displays the simulated

Q, with performance exceeding 10, indicating satisfactory results. The designed SIWs operate adequately and can be used as a substitute for inductors.

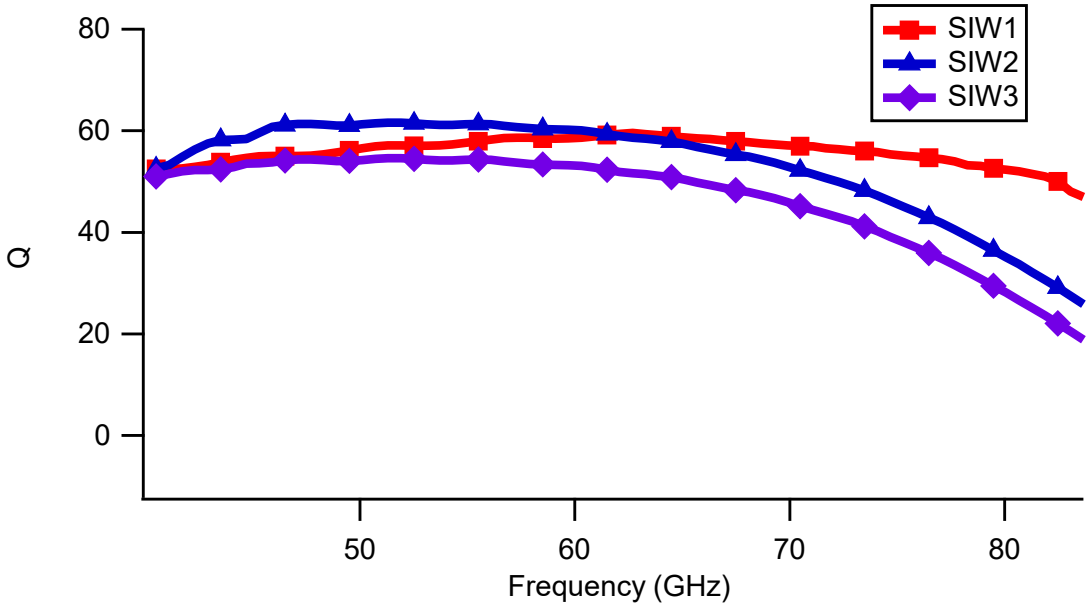

Figure 4.5: Q factor of the designed SIWs

4.2 Diagrammatic Representation of the LNA

The adoption of a wide-band impulse for transmission has streamlined the architecture of the receiver front-end. Nevertheless, the challenges in the design of a UWB LNA persist primarily due to the expansive bandwidth. Despite the extensive research on LNAs in CMOS technology, wide-band RF amplifiers are typically deployed in compound semiconductor technologies due to their superior inherent frequency response and noise characteristics. The CMOS technology's lossy silicon substrate with greater parasitic elements significantly reduces the amplifier's gain and noise performance as frequency rises, therefore limiting the highest attainable bandwidth.

The distributed amplifier (DA) is considered a promising option for wide-band amplification due to its ability to absorb the parasitic capacitances of the active devices across the transmission lines.

Nevertheless, the distributed amplifiers are unable to attain large gain because of the cumulative effect of each transistor's gain. The average strength of the reported DAs is approximately 8 dB, which is inadequate for amplifying the received UWB signal. Conversely, a conventional DA consumes about 60 mW of power, which is excessive for battery-operated portable ultra-wideband equipment [90]. Additionally, while the DA can offer broad-spectrum amplification, it has not been optimized for noise characteristics.

The noise performance of a Low-Noise Amplifier (LNA) is directly influenced by its input impedance matching. Wide-band input matching is inherently noisier than narrow-band counterparts because noise performance cannot be tailored for a given frequency. The tradeoff between achieving wide-band input matching and maintaining a low noise figure in the UWB LNA needs to be thoroughly examined and determined. Figure 4.6 illustrates the four fundamental 50 Ω input matching methods studied in the conventional transistor-amplifier field [91], [92].

The common-gate architecture, also known as the $\frac{1}{g}$ termination, shown in Figure 4.6(c), offers the greatest potential for achieving wide-band input matching. Research on the design of a common-gate LNA has been restricted [91]. This limitation might stem from the fact that conventional narrow-band receivers do not necessitate broad input matching, and a common-gate amplifier often has lower gain and greater noise figure compared to a common-source amplifier.

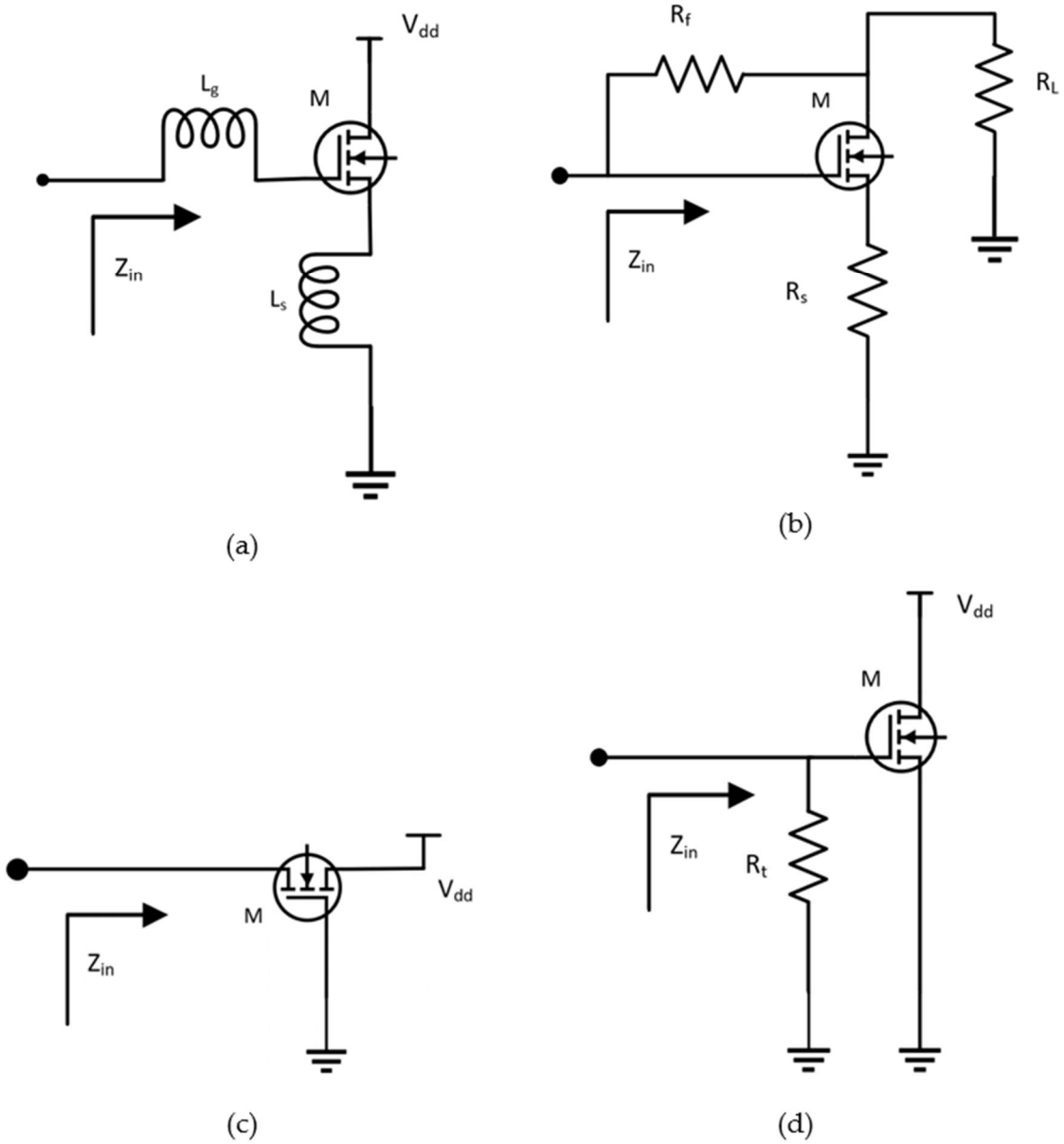

Figure 4.6: Basic input matching techniques (a) Inductive source degeneration (b) Shunt-series feedback (c) Common-gate $\frac{1}{g}$ termination (d) Direct resistor termination

If the input impedance of a common-gate amplifier is predominantly resistive and perfect matching is attained by adjusting the transconductance of the active device to 20 mS, the noise factor (F) can be calculated as –

$$F = 1 + \frac{\gamma}{\alpha R_s g_m} = 1 + \frac{\gamma}{\alpha} \tag{4.8}$$

The MOS transistor's coefficient of channel thermal noise is denoted by γ and is α defined as the ratio of the transconductance and g_{d0} the zero-bias drain conductance, respectively [92].

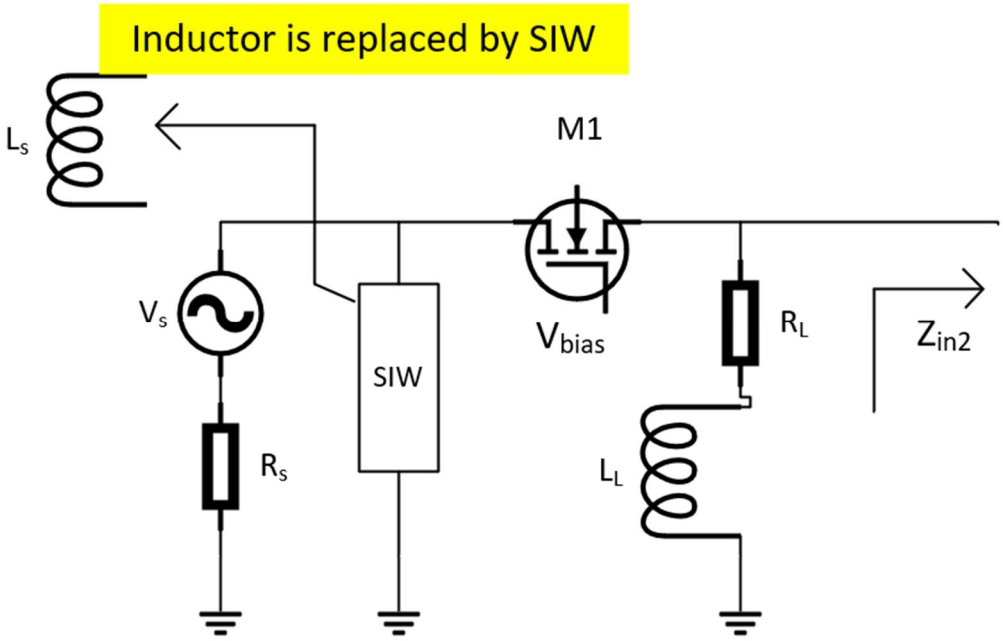

Figure 4.7: Configuration of a common-gate input stage

To enhance noise performance, increase the transconductance of the MOS transistor, even if it means sacrificing the 50 Ω input matching due to its process-dependent and hard-to-control nature.

The common-gate stage's current setup in Figure 4.7 is more intricate than the one seen in Figure 4.6 (c). An SIW is positioned between the MOS transistor's source and the ground terminal to create resonance with the gate-to-source capacitance in a common-gate configuration. The transistor's finite output resistance affects the LNA's performance. Figure 4.7 illustrates the adverse impact on matching and noise performance resulting from the load impedance of the common-gate stage and the input impedance of the subsequent stage. This effect is attributed to the low output resistance of the short-channel MOS transistor, typically around 50 Ω for a 0.18-nm CMOS process [93] – [97].

Another crucial aspect in design is the relatively modest amplification provided by a common-gate amplifier, which contrasts with the aim of achieving high amplification for the received UWB signal. The small-signal model of the transistor used in the analysis, depicted in Figure 4.8, incorporates both the gate-to-drain parasitic capacitance C_{gd} and the finite output resistance R_o. This inclusion allows for an examination of how these significant parasitic elements affect the performance of the proposed LNA.

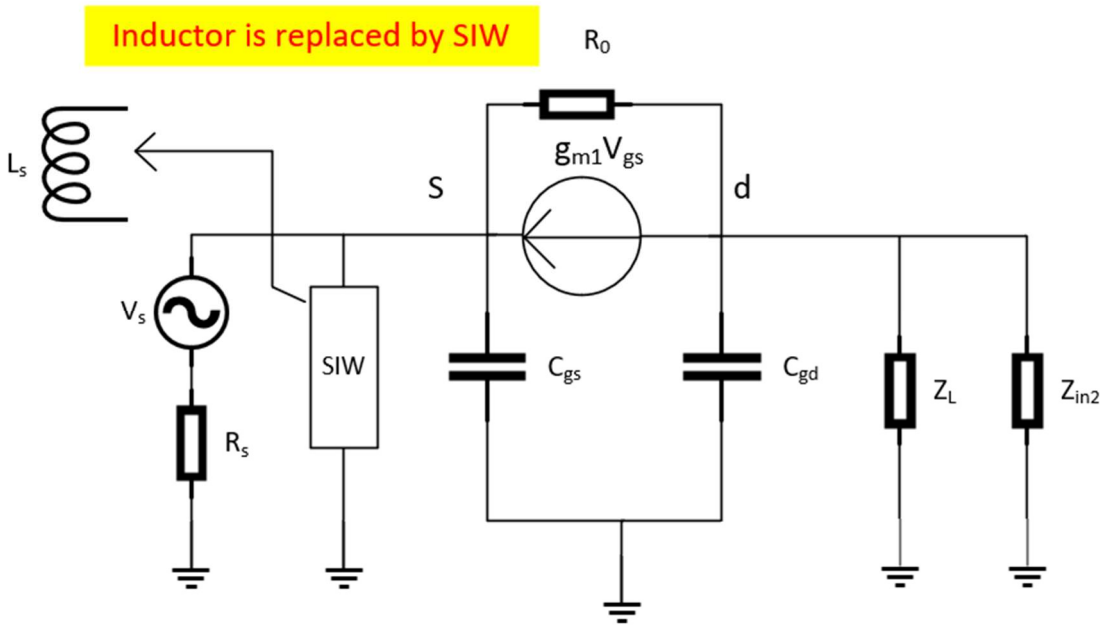

Figure 4.8: MOS transistor small-signal model usages in common-gate stage input impedance derivation

4.2.1 Input matching

Figure 4.8 provides the small-signal equivalent circuit used for calculating impedance. The impedance of the load, the input impedance of the next stage, and the transconductance of the MOS transistor in common-gate arrangement are denoted as, Z_L, Z_{in2} and, g_{m1} respectively. The input impedance can be calculated.

$$Z_{in} = \frac{1}{g_{m1} + \frac{1}{Z_s(\omega)} + \frac{1 - g_{m1}Z_o(\omega)}{R_o + Z_o(\omega)}} \tag{4.9}$$

Where $Z_s(\omega)$ and $Z_o(\omega)$ are given below respectively –

$$Z_s(\omega) = jX_s(\omega) \tag{4.10}$$

$$Z_o(\omega) = jX_o(\omega) \tag{4.11}$$

Equation 4.9 can be re-written as –

$$Z_{in} = \frac{1}{g_{m1} - j\,\frac{1}{X_s(\omega)} + \frac{1 - jg_{m1}X_o(\omega)}{R_o + X_o(\omega)}} \tag{4.12}$$

4.2.2 Gain Analysis and Variable Gain Mechanism

A common practice involves using a resistor as the load for a wide-band amplifier in conjunction with a series inductor to elevate the load impedance at high frequencies. However, employing such a load is unsuitable for a common-gate Low Noise Amplifier (LNA) as the resistor significantly degrades its noise performance. In our design, a SIW is employed as the load, impacting the overall capacitance at the output of the common gate stage and constraining the amplifier's bandwidth. To overcome this limitation, this study introduces an innovative approach aimed at enhancing the bandwidth and amplifying the gain of the amplifier. The introduction of a common-source stage with SIW after the common-gate stage serves to improve the overall gain of the amplifier. The selection of SIW is guided by resonance with the total capacitance at the output terminal. Optimizing the frequency points results in an enhanced bandwidth and gain for the amplifier.

4.2.3 Noise Analysis and Optimization

The noise characteristics of the proposed Low Noise Amplifier (LNA), which incorporates a common-gate stage for wide-band input matching, require meticulous consideration due to its propensity to manifest higher noise levels

compared to narrow-band matching approaches like inductive source degeneration.

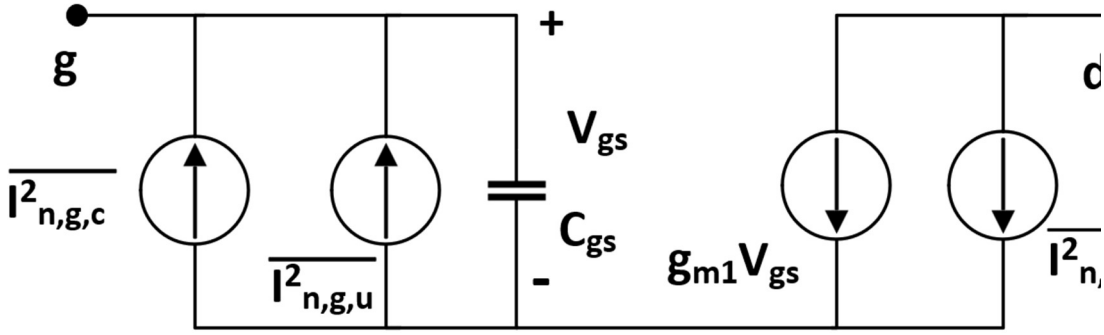

Figure 4.9: MOS transistor noise model including the induced gate noise

The analysis employs the MOS transistor noise model, encompassing induced gate noise and channel thermal noise, to enhance noise performance has shown in Figure 4.9) [98]. Figure 4.9 shows the average power spectral density (PSD) of the channel thermal noise labeled as $\overline{\iota^2_{n,d}}$.

$$\frac{\overline{\iota^2_{n,d}}}{\Delta f} = 4kT\gamma g_{d0} \tag{4.13}$$

The variables in question are k (Boltzmann constant), T (absolute temperature in Kelvin), g_{d0} (zero bias drain conductance), and Δf (bandwidth over which the noise figure is measured) [97] – [99]. The Power Spectral Density (PSD) of the gate noise that is produced is provided –

$$\frac{\overline{\iota^2_{n,g}}}{\Delta f} = 4kT\delta g_g \tag{4.14}$$

Where δ is the coefficient of the induced gate noise and g_g is the equivalent shunt gate conductance, which is given by $g_g = \frac{\omega^2 C_{gs}^2}{5g_{d0}}$. Typically, δ is $\frac{4}{3}$ for long-channel devices, and it increases in short-channel devices [97] – [99].

The determination of the noise factor for the common-gate input stage, followed by a common-source stage, is achievable. –

$$F = F_1 + \frac{S_{n,g,u,2}}{S_{n,R_s}} + \frac{S_{n,g,d,c,2}}{S_{n,R_s}} \tag{4.15}$$

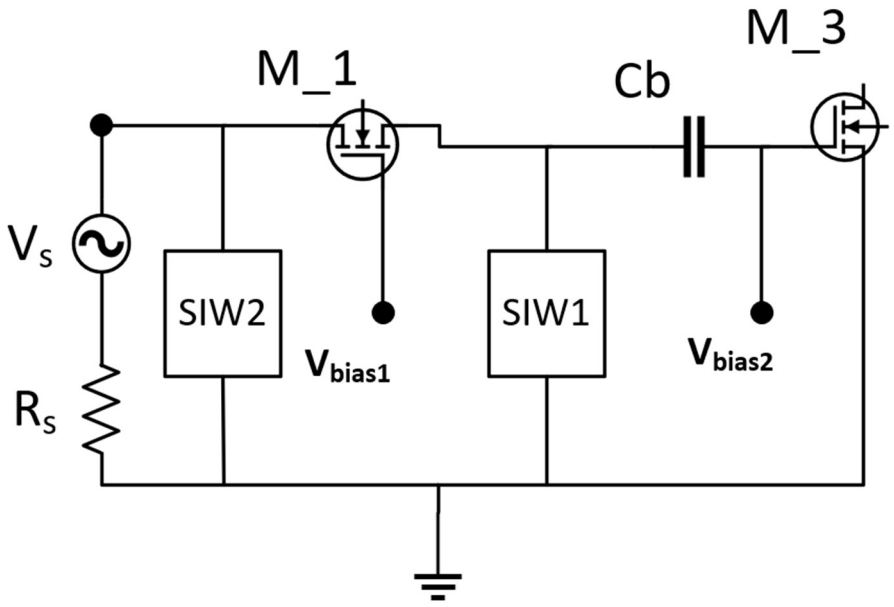

Figure 4.10: Noise calculation of the common-gate stage cascaded by a common source stage

Because the common-gate stage has limited amplification, we cannot overlook the noise contribution from the following stages. To achieve a more precise estimate of the amplifier's noise performance, we calculate the noise figure at the output of the second common-source stage. This calculation is based on the circuit schematic provided in Figure 4.10, which illustrates the circuit for noise analysis along with its small signal equivalent.

F_1 represents the noise factor of the single common-gate stage, excluding the noise contributed by the common-source stage, as denoted by the final two terms. The formula for F_1 is given as:

$$F_1 = 1 + \frac{\alpha\delta.(1-|C|^2).\omega^2 C_{gs1}^2 R_s}{5.g_{m1}} + \frac{\gamma}{\alpha R_s g_{m1}}\left(1 + \frac{R_s^2}{|Z_s(\omega)|^2}\right) + \frac{\alpha\delta|C|^2 C_{gs1}^2 R_s}{5.g_{m1}} + \frac{2|C|\sqrt{\frac{\delta\gamma}{5}}\omega C_{gs1} R_s}{j g_{m1} Z_s(\omega)} \quad (4.16)$$

Two methods can be used to reduce the noise figure, as shown in equation 4.16.

i. The inductance values of SIW2 and C_{gs1} can be adjusted to resonate at the center of the chosen frequency band to achieve a maximum $|Z_s(\omega)|$ at that frequency and optimize the average $|Z_s(\omega)|$ value throughout the whole bandwidth. This aligns with the need for proper matching of inductance in SIW2 and C_{gs1}, as previously mentioned.

ii. Since g_{m1} is present in the denominators of all noise components, increasing it can help decrease the total noise. Yet, the accuracy of the input matching diminishes as g_{m1} grows.

4.3 Schematic of the Proposed LNA

Figure 4.11 displays the schematic of the common gate (CG) LNA. The size of the M_1 transistor is selected to ensure sufficient transconductance (g_{m1}) for input power matching. Equation 4.17 can be used to calculate the input impedance of the LNA.

$$Z_{IN} = \frac{1}{g_{m1}} \quad (4.17)$$

The second stage, called common source (CS) structure, and the third stage, referred to as common gate, function together as a noise cancellation stage. The CS stage is known for its low noise figure (NF), wideband capabilities, low parasitic capacitance, and high gain, which reduces the impact of thermal noise from the M_3 transistor. The noise canceling stage eliminates out-of-phase input

voltage noise from the previous stage and combines the in-phase voltage signal at the output node.

Current mirror circuits are utilized for transistor biasing. To correctly ground the AC and prevent noise from the biasing circuit, a 400 fF capacitor is connected between the gate and the ground line. The particular requirements for the LNAs are outlined in Table 4.2.

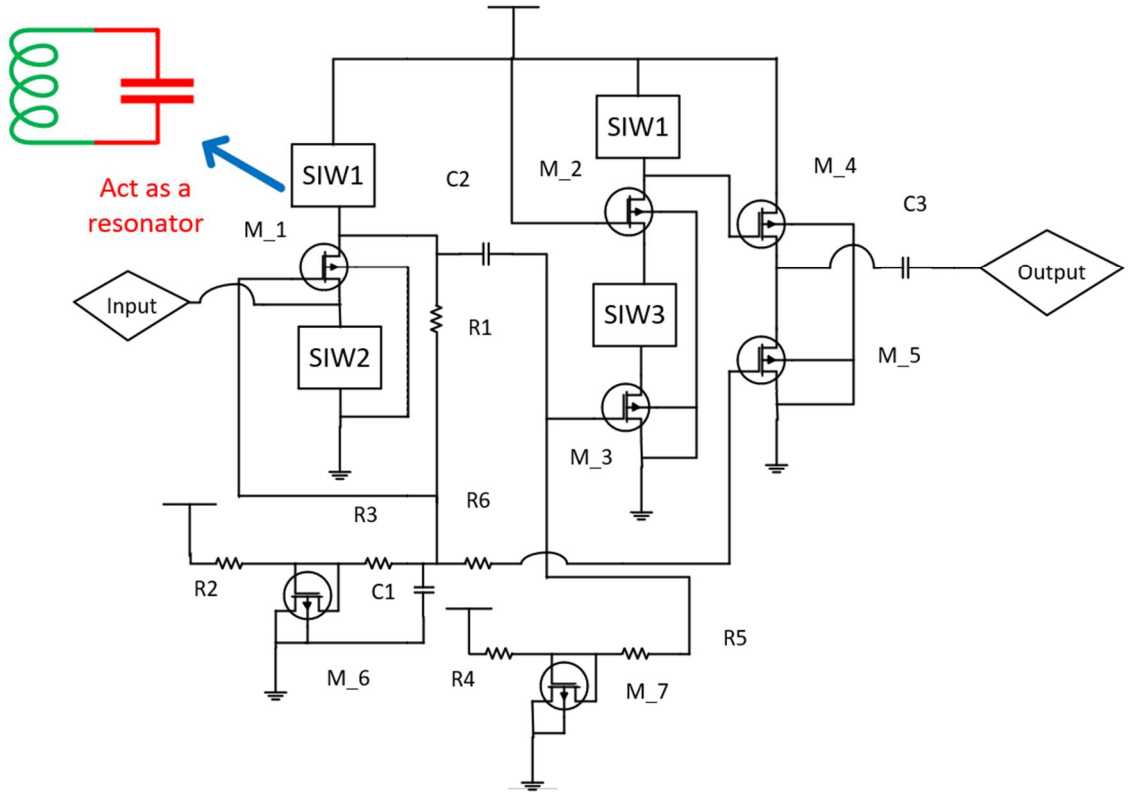

Figure 4.11: Schematic diagram of the proposed LNA

SIW1 is designed to resonate with capacitances C_{gd} and C_{gs} in a certain frequency range, emphasizing the need to choose a suitable width for M_3. Iterative calculations show that SIW1 is designed with a width of M_3 at 60 µm to achieve optimal noise performance.

M_1 and M_3 have distinct aspect ratios, however SIW1 and SIW2 are engineered to maintain identical resonant frequencies for the LC tanks created by the inductance of SIW2 with C_{gs} and SIW1 with C_{gs3}+ C_{gd} . The issue is caused

by the presence of C_{gd1} and the parasitic capacitance introduced by coupling capacitor C2.

Table 4.2: Dimensions of the Proposed LNAs

MOSFET	**M_1 (μm)**	**M_2 (μm)**	**M_3 (μm)**	**M_4 (μm)**	**M_5 (μm)**	**M_6 (μm)**	**M_7 (μm)**
	90	90	60	60	120	240	80
Capacitor	**C1 (fF)**	**C2 (pF)**	**C3 (pF)**				
	400	15	15				
Resistor	**R1 (kΩ)**	**R2 (kΩ)**	**R3 (kΩ)**	**R4 (kΩ)**	**R5 (kΩ)**	**R6 (kΩ)**	
	3.5	5	0.5	5	5	0.5	

Table 4.2 provides us the optimized value of the used components which makes a trade-off between all performance parameters. A source-follower has been incorporated as an output buffer for testing. Z_m is the impedance of the LC tank formed by the inductance of SIW1. The output impedance is the sum of C_{gd2} and C_{gd4}.

$$Z_o \approx \frac{1 + j\omega Z_m(\omega) C_{gs4}}{g_{m4} + j\omega C_{gs4}} \tag{4.18}$$

SIW1 is chosen to maximize the peak to prevent degradation of in-band output matching. Transistor M_4 functions as a source follower with a width of 60 μm to reduce the influence of C_{gs4}.

Current mirrors are used for circuit biasing. Both the single stage and common-gate stage employ a current mirror to bias the source-follower and reduce power usage. Resistors R3, R5, and R6, in conjunction with capacitor C1, create a LP filter to provide adequate reverse isolation. To change the overall amplification of the LNA, vary the resistance value of R4 by considering the biasing current and transconductance of the single stage. A reduced C_{gs} will lead

to a decreased noise figure. Increasing the current requires a decrease in the width of M_1 to retain the same g_{m1}. The M_1 width is selected to be maximized within acceptable noise performance standards.

The design of LNA involves an iterative procedure to achieve the desired performance. LNA performance parameters exhibit tradeoffs. The LNA design involves multiple optimization criteria.

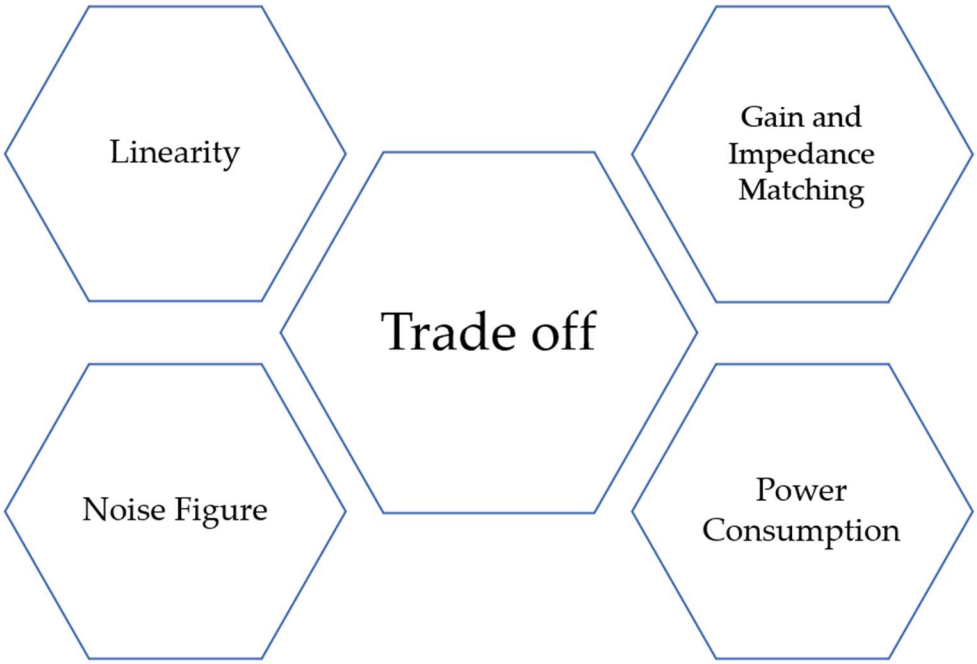

Figure 4.12: Performance trade-off of LNA

Figure 4.12 illustrates the trade-offs in electronic system design, particularly for amplifiers. It shows that optimizing parameters like linearity, noise figure, gain and impedance matching, and power consumption are interdependent. Enhancing one often comes at the expense of another: for example, improving linearity might increase power consumption, while reducing noise might decrease gain. Designers must balance these factors to achieve the desired overall performance, finding an optimal compromise based on the specific requirements of the application.

4.4 Design Optimization

In the realm of nanoscale design, the manual determination of optimal values for design variables becomes a formidable and impractical task, primarily owing to the intricate mathematical model characterizing Metal-Oxide-Semiconductor Field-Effect Transistors (MOSFETs). The complexity inherent in the mathematical representation of MOSFET behavior renders the manual optimization of design variables challenging and time-prohibitive.

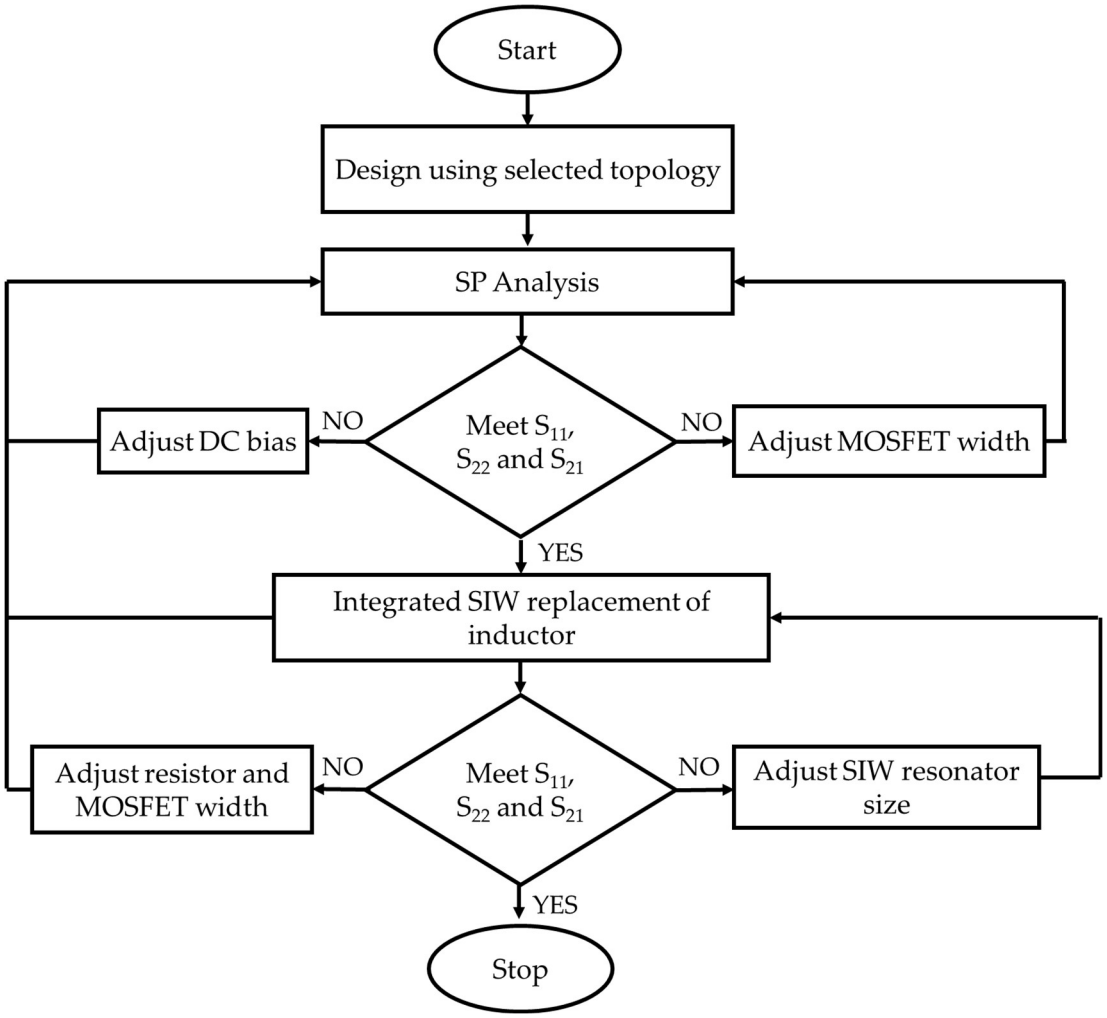

Figure 4.13: LNA design flow chart

Consequently, optimization algorithms emerge as indispensable tools in the identification of optimal variable values, offering a computational approach to address the intricacies associated with nanoscale design. Illustratively, Figure

4.13 provides a visual representation in the form of a flow chart, elucidating the systematic process involved in design optimization.

In simpler terms, when working with extremely small-scale designs like nanotechnology, it's really hard and almost impossible to manually figure out the best values for the design elements because of the complicated math behind MOSFETs. To tackle this challenge, we commonly use optimization algorithms. These algorithms help us find the best values for our design variables without spending a lot of time and effort. Figure 4.13 is like a roadmap that shows the step-by-step process of how we use these algorithms to optimize our designs.

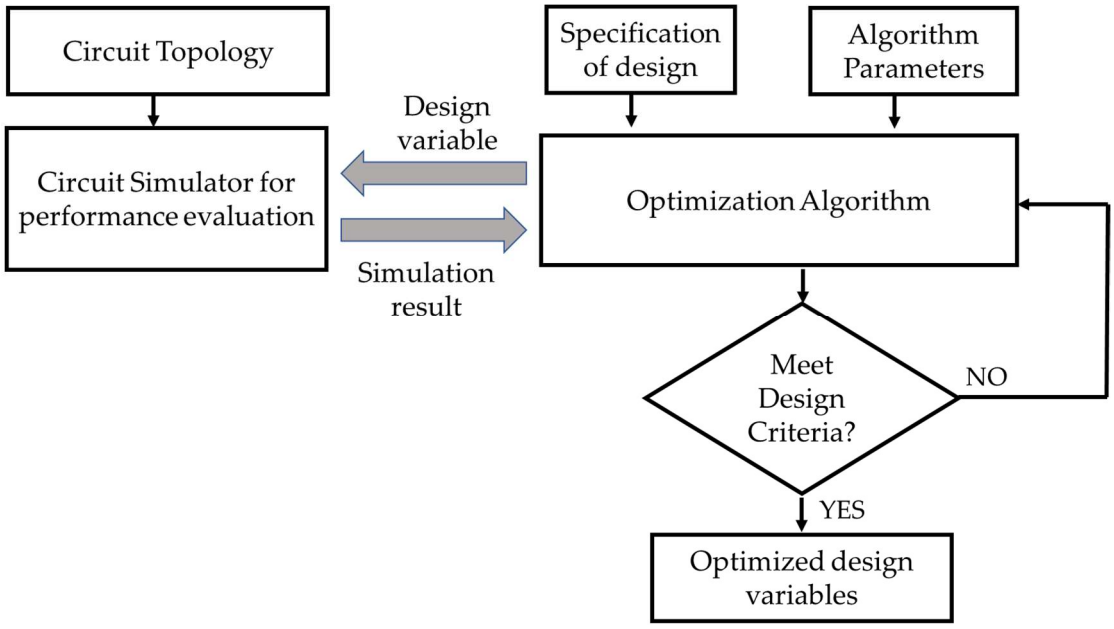

Figure 4.14: LNA design optimization flow chart

Figure 4.14 represents the design optimization process in electronics, emphasizing the trade-offs necessary to achieve better performance. It shows two parameters, "Performance" and "Efficiency," connected by bidirectional arrows, indicating that improving one often affects the other. Optimizing design requires balancing these parameters; enhancing performance might reduce efficiency and vice versa. The arrows signify the need for a careful, iterative approach to find an

optimal compromise that meets the specific design goals while managing the interdependencies between performance and efficiency.

4.5 Simulation Result and Discussion

Cadence is employed for simulating circuits in the proposed design. Figure 4.15 illustrates the input reflection coefficient and output matching of the recommended LNA. The bandwidth consistently remains at – 10 dB for S_{11} and S_{22}, indicating a favorable correlation between the input and output.

Getting the right impedance match is crucial when designing radiofrequency amplifiers. It helps improve performance and maintains signal quality. After thorough investigation, we found that the best input impedance match occurs at around – 14.4 dB, and the top output impedance match is – 15.09 dB, both at a frequency of 69 GHz. This emphasizes that impedance matching depends on the specific frequency.

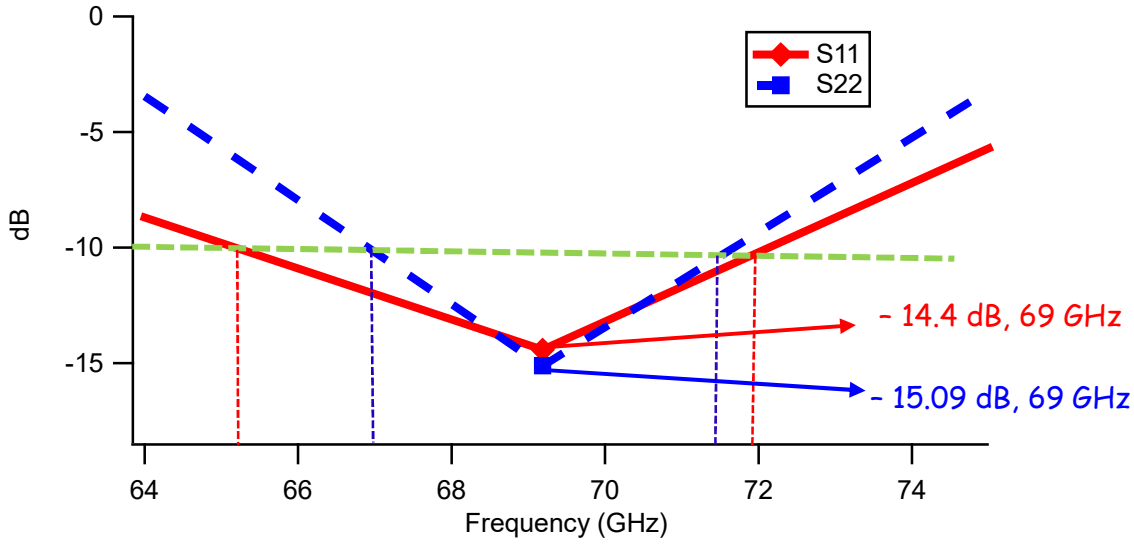

Figure 4.15: Input reflection coefficient and output matching

Figure 4.16 visually presents this insight, showing gain curves from detailed simulations of the suggested Low-Noise Amplifier (LNA). The graph gives a clear picture of how the gain changes with different frequencies. The gain

noticeably increases as the frequency goes up, highlighting the amplifier's effectiveness in amplifying signals across the electromagnetic spectrum. This emphasizes how important frequency considerations are in determining how well the amplifier works. So, having impedance matching tailored to the frequency is crucial for optimizing the LNA's performance.

To sum it up, the detailed impedance matching characteristics at 69 GHz, illustrated in Figure 4.16, provide a thorough understanding of how the amplifier behaves. This information is valuable for designers looking to refine and optimize radiofrequency amplifier designs.

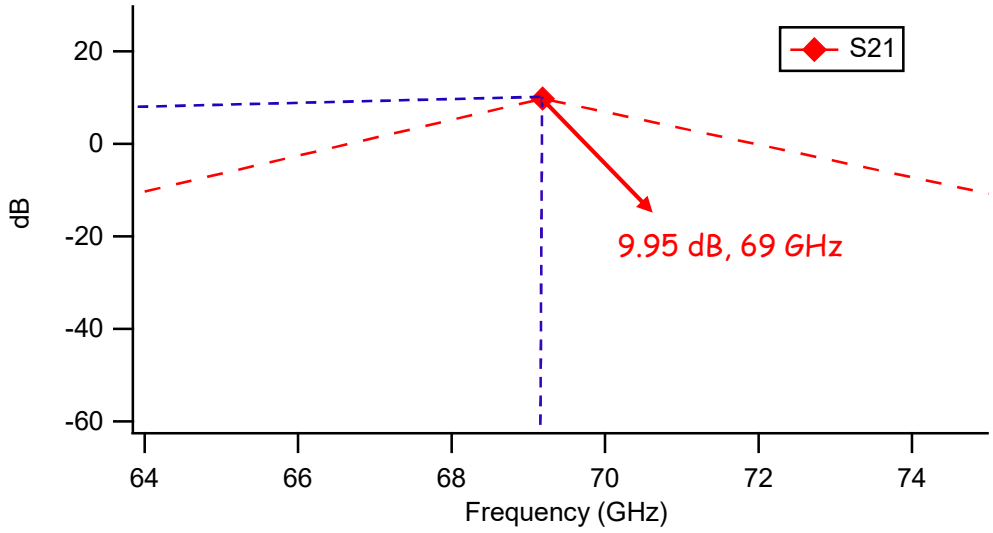

Figure 4.16: Gain of the proposed LNA

The gain characteristics of the examined system manifest notable disparities across distinct frequencies, underscoring the nuanced nature of its performance. Specifically, the gain is observed to approximate 1.4 dB at a frequency of 67 GHz, experiencing a discernible augmentation to approximately 9.95 dB at 69 GHz. Furthermore, a subsequent transition is noted as the gain converges to around 1.56 dB at the elevated frequency of 71.5 GHz.

A pivotal component instrumental in the fine-tuning of the gain attributes is the resistor denoted as R4. The judicious adjustment of this resistor facilitates an independent modification of the transconductance (g_m) within the singular

amplification stage. This nuanced control, in turn, engenders a meticulous regulation of the overall gain exhibited by the Low-Noise Amplifier (LNA). The capacitive integration of R4 within the system architecture thereby imparts a level of precision and granularity to the gain manipulation process, affording the practitioner a discernible degree of control over the system's amplification dynamics.

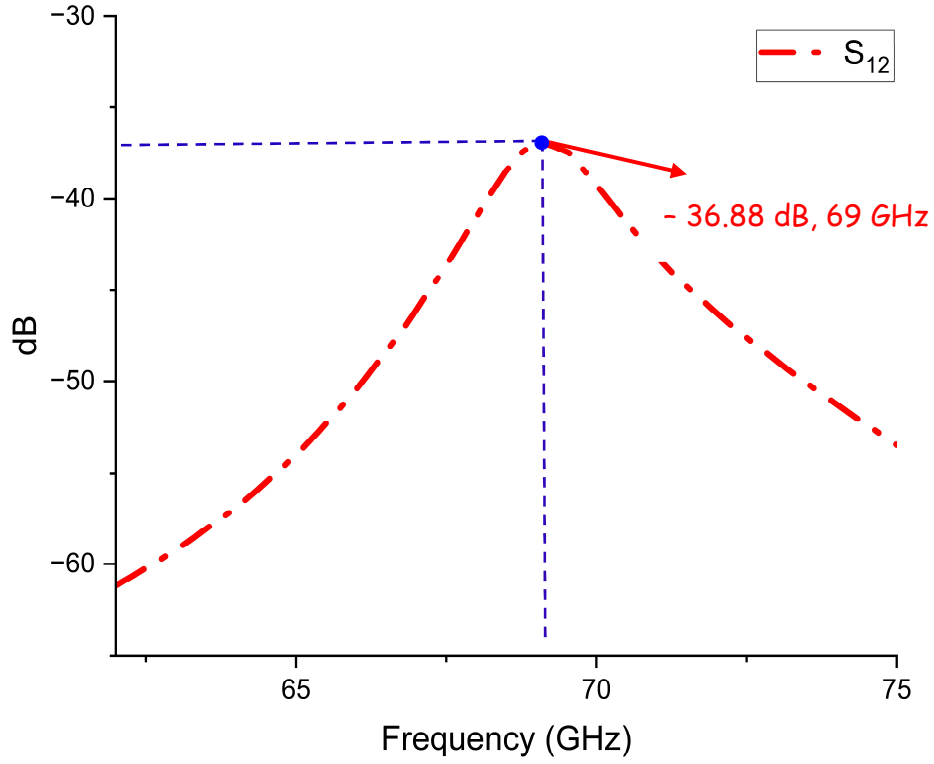

Figure 4.17: Isolation of the proposed LNA

This delineation elucidates the intricate interplay between circuit elements and the resultant impact on the gain profile, accentuating the significance of resistor R4 in tailoring the performance characteristics of the single-stage amplifier within the broader context of the LNA design.

The inherent attribute under consideration serves to expedite alterations in the architectural configuration when a precise gain value is necessitated for the Low-Noise Amplifier (LNA). Illustratively, Figure 4.18 elucidates the noise performance characteristics inherent in the proposed design. At a frequency of

69 GHz, the minimum discernible noise level attains a value of 8.33 dB. This noise floor exhibits a discernible variability across a spectrum of frequencies, extending from the lower to the upper bounds. Remarkably, the pinnacle of the noise figure is realized at 11.77 dB, manifesting at a frequency of 71.5 GHz within the prescribed frequency range.

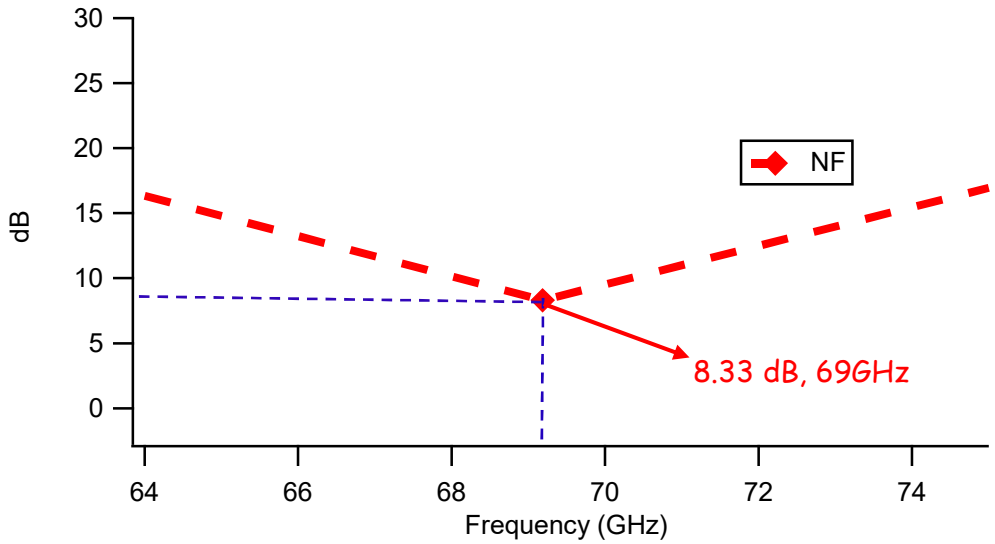

Figure 4.18: Noise figure of the proposed LNA

SIW automatically decreases transmission losses and enhances isolation between input and output. The particular geometric characteristics of Substrate Integrated Waveguide (SIW) enhance the performance of S_{11} and S_{22}.

Figure 4.19 shows the layout of the LNA. The numerical data indicates that the SIW-based LNA has better S_{11} and S_{22} values than inductor-based LNAs. SIW has natural traits that enable a wider frequency range. Dispersed components can function over a wide range of frequencies due to their topological features. Reduced losses from utilizing substrate integrated waveguides result in an increased bandwidth.

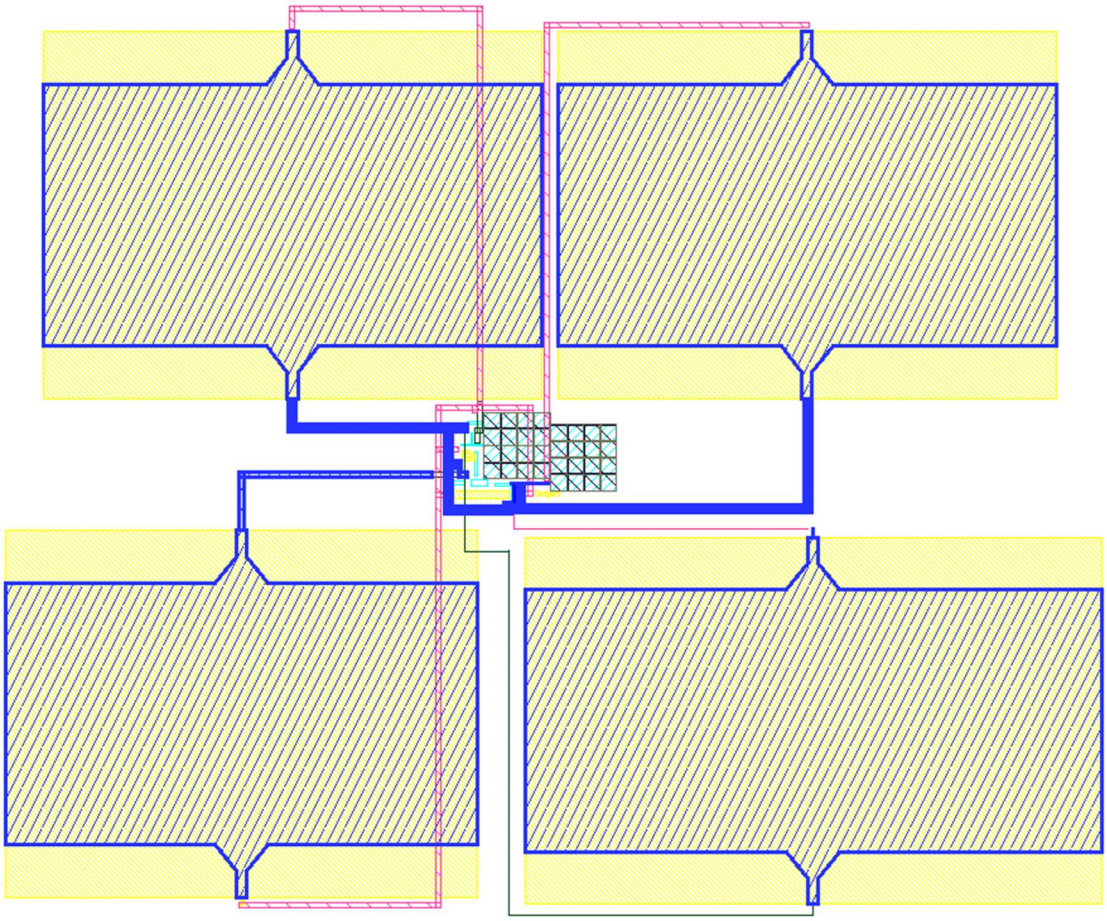

Figure 4.19: Layout of the proposed LNA

The table 4.3 compares CMOS amplifiers across various studies, detailing their technology node, operating frequency, bandwidth, gain, input and output reflection coefficients, noise figure, and topology. It shows that smaller technology nodes 0.065 μm tend to operate at higher frequencies 62 GHz with wider bandwidths 10 GHz and higher gain 21.5 dB, but may also exhibit higher noise figures 6.7 dB. In contrast, older technology nodes 0.18 μm often operate at lower frequencies 2.4 GHz with narrower bandwidths 1 GHz and lower gain 12.68 dB, but can have better noise performance 2.85 dB. The table also highlights different topologies, such as cascode and inductor configurations, and their impact on performance metrics like gain and noise figure. The proposed inductor less LNA operates in the frequency range of 67.5 GHz to 71.5 GHz, strategically aligning with the 180 nm technology transition frequency (fT).

Table 4.3: Comparison of this work with recent works

Source	CMOS Technology (μm)	Resonance Frequency (GHz)	BW (GHz)	S_{21} (dB)	S_{11} (dB)	S_{22} (dB)	NF (dB)	Topology
[77]	0.09	68	4	20.2	< - 11	< - 16	8.8	1 CS + 2 cascode + inductor
[78]	0.065	62	10	21.5	< - 8	< - 9	6.7	4 stage cascode + inductor
[61]	0.18	7.2	1	17.2	< - 15	< - 12	2.85	1 stage + inductor
[62]	0.18	2.4	1	12.68	< - 13.5	< - 10	3.14	2 stages + inductor
[79]	0.18	8	10	15.02	< - 9.4	< - 15.8	4.4	FB resistor + LG inductor
[81]	0.18	3	5	12.5	< - 10	< - 11	4.5	Balun LNA
This Work	0.18	69	4.5	9.95	< - 14.4	< - 18.6	8.33	1 stage + SIW (without inductor)

The distinct high-quality factor (Q) characteristic inherent in SIW resonators is harnessed to achieve a commendable gain ($|S_{21}|$) at the designated operating frequencies. The judicious incorporation of the noise canceller circuit not only maintains an excellent input match ($|S_{11}| < -14$ dB) and output match ($|S_{22}| < -15$ dB) but also contributes to an average noise figure of 8.3 dB and a power gain of 9.76 dB at 69 GHz. The significance of this work extends beyond the mere introduction of an inductor-less SIW-based LNA. The utilization of SIW

resonators brings forth a technological milestone in CMOS LNA design. By eliminating the active spiral inductor, the proposed LNA achieves a delicate balance between gain, noise performance, and frequency compatibility. This research represents a breakthrough, opening new avenues for the application of SIW in high-frequency electronics and advancing the frontiers of CMOS LNA design.

5 Conclusions & Future Work

5.1 Conclusions and Major Contribution

In the pursuit of advancing wireless communication technologies, this thesis embarked upon the design and analysis of a UWB Low Noise Amplifier (LNA) employing a Substrate Integrated Waveguide (SIW) resonator within the framework of a 180 nm technology. The overarching objective was to propel RF receiver performance to meet the evolving demands of future wireless communications. The attainment of this objective required a meticulous exploration of key components and trade-offs inherent in the design process.

The initial goal of this study was to create and enhance a Substrate Integrated Waveguide (SIW) resonator to reach the necessary resonance frequency while maintaining optimal performance. The SIW resonator is a key component in the system's architecture, improving its resonance qualities. The resonator was customized to satisfy specific requirements by thorough study and repeated improvements, becoming a key component in the next design phases. The imaginary component of the impedance of the designed substrate integrated waveguides is constant. States that the inductance value is constant at higher frequencies. A spiral inductor exhibits resistive behavior at higher frequencies. Substitute SIW with an inductor to improve performance.

The second goal was to include the SIW resonator into the design of a Low Noise Amplifier (LNA) customized for Ultra-Wide Band (UWB) wireless receivers. This integration sought to utilize the SIW resonator's characteristics to obtain increased gain, decreased noise figure, and a wider bandwidth. The strategic integration of the SIW resonator with the LNA architecture was crucial in achieving improved performance metrics. The design successfully combined

state-of-the-art SIW technology with LNA functionality, expanding the limits of traditional RF receiver capabilities.

This research extensively examined the performance of the suggested LNA. The study involved a thorough analysis of important factors such as gain, noise figure, and bandwidth. The recommended Low-Noise Amplifier demonstrated exceptional results in Ultra-Wideband wireless communication systems based on simulations and empirical validations. – 14.4 dB is the maximum input impedance matching value and – 15 dB is the maximum output impedance matching value at 69 GHz. The gain varies 1.4 dB to 9.95 dB to 1.56 dB where the frequencies are at 67 GHz, 69 GHz, and 71.5 GHz. The noise level is at a minimum of around 8.33 dB at 69 GHz.

5.2 Implications and Future Directions

The integrated CMOS UWB LNA is a major step towards developing single-chip UWB transceivers. The suggested methodology eliminates the requirement for high spiral inductors, simplifying the design process and demonstrating its suitability for wide-band designs in CMOS technology. This study suggests opportunities for more research in incorporating cutting-edge technologies to improve the functionalities of UWB transceivers, leading to the development of more effective and smaller wireless communication systems.

In conclusion, the thesis has successfully achieved its aims and made a significant contribution to the field of UWB wireless communication. Incorporating SIW resonator technology into the UWB LNA design showcases the possibility of improving receiver performance. As we approach a new era in wireless communication, the knowledge acquired from this research establishes a strong basis for future projects in creating advanced, integrated UWB transceivers.

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