Hardware-Software Codesign of Electrooculogram Signal Processors

By

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A thesis submitted in partial fulfillment of the requirements for the degree of MASTER of SCIENCE in Electrical and Electronic Engineering

Department of Electrical and Electronic Engineering

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Dedication

To my family members for their continuous support

List of Publications

Journal Article

- Publication 1: **Diba Das**, Aditta Chowdhury, Abdurrashid Ibrahim Sanka, Ray C. C. Cheung, Quazi Delwar Hossain, and Mehdi Hasan Chowdhury, "Electrooculogram Based Point of Care Systems: A Systematic Review ", *SN Computer Science*. **(Under review)**

- Publication 2: **Diba Das**, Mehdi Hasan Chowdhury, Aditta Chowdhury, Kamrul Hasan, Quazi Delwar Hossain, and Ray C. C. Cheung, "Application Specific EOG Processor for Blink Detection", *Journal of Low Power Electronics and Applications*. **(Under review)**

- Publication 3: **Diba Das**, Aditta Chowdhury, Ray C. C. Cheung, Quazi Delwar Hossain, and Mehdi Hasan Chowdhury, "EOG Signal Processor: A Multiclass Classifier to Detect Eye Movements", *Journal of Signal Processing Systems*. **(Under review)**

Conference

- **Diba Das**, Aditta Chowdhury, Abdurrashid Ibrahim Sanka, and Mehdi Hasan Chowdhury, "Design and Performance Evaluation of an FPGA based EOG Signal Preprocessor," 2023 International Conference on Electrical, Computer and Communication Engineering (ECCE), Chittagong, Bangladesh, 2023, pp. 1-6. **(Published)**

Approval by the Supervisor

This is to certify that Diba Das has carried out this work under my supervision and that she has fulfilled relevant Academic Ordinance of the Chittagong University of Engineering and Technology, so that she is qualified to submit the following thesis in application for the degree of MASTER of SCIENCE in Electrical and Electronic Engineering

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Abstract

Electrooculogram (EOG) is a bioelectric signal carrying eye movement information. This signal can be utilized in medical and bio-electrical applications such as diagnosing different ocular diseases and controlling human-computer interfaces. Point of care (POC) systems refer to the systems where testing is performed right where the patient is. POC systems dedicated to detecting various eye conditions can be developed by hardware implementations of EOG. Field Programmable Gate Arrays (FPGAs) are reconfigurable integrated circuits offering flexible software features with fast parallel computation. Application specific designs in FPGA fix the functionality and reduce the number of components used providing cost-effectiveness, and power efficiency. In this research, a systematic investigation of the research trend on hardware implementations of EOG is presented first. After that, an in-depth analysis of two novel FPGA-based architectures is presented. The first work aims to design a hardware-optimized binary EOG processor for blink detection by using multichannel EOG signals containing horizontal and vertical EOG signals. After preprocessing the EOG signals, by extracting only two features- root mean square (RMS) and standard deviation (STD), blink and saccades are classified employing support vector machine (SVM) with 97.5% accuracy. The implemented system of this design in Xilinx Zynq-7000 FPGA achieves an accuracy of 95%. The second work aims to design a hardware-optimized machine learning based EOG signal processor to classify six different eye movements (up, down, normal, right, left, and blink) adopting an SVM classifier with average software accuracy of 97.92%. The accuracy of the implemented system in Zynq UltraScale+ is 95.56%. The efficacy of the developed systems is proved by comparing them with state-of-the-art technologies. A few potential future research scopes are mentioned at the end of the thesis.

সারাংশ

ইলেক্ট্রোকুলোগ্রাম (EOG) সিগন্যাল হল একটি জৈব বৈদ্যুতিক (Bio-electric) সংকেত যা চোখের গতিবিধির তথ্য বহন করে। এই সিগন্যাল চিকিৎসা এবং জৈব বৈদ্যুতিক অ্যাপ্লিকেশনে ব্যবহার করা যেতে পারে, যেমন চোখের বিভিন্ন রোগ নির্ণয় করা এবং মানব-কম্পিউটার পরিচালনা নিয়ন্ত্রণ করা। তাৎক্ষনিক সেবা কেন্দ্র (Point-of-Care System) রোগীর অবস্থানেই পরীক্ষা সম্পাদন করে। হার্ডওয়্যারে EOG সিগন্যাল বাস্তবায়ন করে তাৎক্ষনিক সেবা কেন্দ্র তৈরি করা সম্ভব, যা চোখের বিভিন্ন রোগ সনাক্তকরণের করতে সক্ষম। ফিল্ড প্রোগ্রামেবল গেট অ্যারে (FPGA) হলো পুনর্বিন্যাসযোগ্য ইন্টিগ্রেটেড সার্কিট যার অন্যতম বৈশিষ্ট্য দ্রুত গণনা। FPGA -এর মাধ্যমে নির্দিষ্ট কাজের জন্য ডিজিটাল সার্কিট ডিজাইনের মাধ্যমে প্রয়োজনীয় উপকরণের সংখ্যা কমানো যায়। এর ফলে, ব্যায় কমে, এবং শক্তি খরচ কম হয়। এই গবেষণায় সর্বপ্রথমে পূর্ববর্তী EOG এর হার্ডওয়্যার বাস্তবায়নের উপর একটি পদ্ধতিগত পর্যালোচনা ও বিশ্লেষণ করা হয়েছে। এরপর, FPGA-ভিত্তিক দুইটি পৃথক সিস্টেম ডিজাইন করা হয়েছে। প্রথম সিস্টেমের লক্ষ্য হলো EOG সিগন্যাল ব্যবহার করে চোখের পলক ফেলা সনাক্তকরণ। এই কাজে দুই চ্যানেল বিশিষ্ট EOG সিগন্যাল ব্যাবহার করে একটি হার্ডওয়্যার এর জন্য উপযোগী দুই শ্রেণীর EOG সিগন্যাল প্রসেসর ডিজাইন করা হয়েছে। মেশিন লার্নিং পদ্ধতি অনুসারে এই সিগন্যালকে প্রিপ্রসেসিং করার পর, দুইটি বৈশিষ্ট্য -রুট গড় বর্গক্ষেত্র (RMS) এবং স্ট্যান্ডার্ড ডেভিয়েশন (STD) নির্ণয়ের মাধ্যমে চোখের পলক ফেলা সনাক্তকরণ করা হয়েছে,। সাপোর্ট ভেক্টর মেশিন (SVM) এই কাজে ৯৭.৫% নির্ভুলতা অর্জন করে। FPGA Zynq-7000 বাস্তবায়িত এই ডিজাইনটি ৯৫% নির্ভুলতা অর্জন করে। দ্বিতীয় কাজের লক্ষ্য একটি হার্ডওয়্যার এর জন্য উপযোগী মেশিন লার্নিং ভিত্তিক EOG সিগন্যাল প্রসেসর ডিজাইন করা। এই কাজে চোখের ছয়টি ভিন্ন গতিবিধি (উপর, নিচে, স্বাভাবিক, ডান, বাম, এবং পলক ফেলা) SVM পদ্ধতিতে ৯৭.৯২% নির্ভুলতার সাথে শ্রেণীবিন্যাস করা সম্ভব হয়েছে। Zynq UltraScale+-এ বাস্তবায়িত এই ডিজাইনে ৯৫.৫৬% নির্ভুলতা অর্জন করা সম্ভব হয়েছে। অত্যাধুনিক প্রযুক্তির সাথে তুলনা করার মাধ্যমে এই গবেষণার কার্যকারিতা নির্ধারণ করা হয়েছে। থিসিসের শেষ অংশে কয়েকটি সম্ভাব্য ভবিষ্যত গবেষণা সম্বন্ধে সংক্ষিপ্ত আলোচনা করা হয়েছে।

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Nomenclature

Abbreviations

BRAM = Block Random Access Memory

CPLD = Complex Programmable Logic Device

DSP = Digital Signal Processor

EEG = Electroencephalogram

EMG = Electromyogram

EOG = Electroculogram

FF = Flipflop

FN = False Negative

FP = False Positive

FPGA = Field Programmable Gate Array

LUT = Lookup Table

LUTRAM = Lookup Table Random Access Memory

RMS = Root Mean Square

RSE = Root Squared Error

POC = Point of Care

SoC = System on chip

SPLD = Simple Programmable Logic Device

STD = Standard Deviation

SVM = Support Vector Machine

TN = True Negative

TP = True Positive

XSG = Xilinx System Generator

List of Symbols

b = Bias

f = Frequency

μ = Mean

σ = Standard Deviation

$\mathbf{x}$ = Feature Vector

$\mathbf{W}$ = Vector containing Weights of Features

C_n = Output of Classifier n

Chapter 1: Introduction

Electrroculogram (EOG) is an electrophysiological signal. This signal provides insights into eye movement patterns and eye-related conditions. EOG-based digital systems can assist people in various fields such as medical professionals, researchers, and developers working on assistive technologies and human-computer interaction. Domain-specific reconfigurable signal processors like field programmable gate arrays (FPGAs) are often desirable in such applications to ensure real-time signal analysis, resource optimization, and point-of-care usage. In this research, state-of-the-art EOG signal processors are thoroughly studied to identify contemporary research dynamics. In this thesis, two novel prototypes are designed to answer a few research questions found in the academic literature. This chapter gives a brief review of EOG signals, EOG data acquisition methods, and various eye movements. An overview of FPGA is also discussed. This chapter outlines the background in Section 1.1, the present state of the problem in Section 1.2, and specific objectives in Section 1.3. Section 1.4 describes the significance and scope of this research. Finally, Section 1.5 includes an outline of the remaining chapters of the thesis.

1.1 Background

According to the World Health Organization (WHO), at least 1 in 6 people go through disability [1]. People from low-income countries are suffering more than others in this issue. WHO introduced the Global Cooperation on Assistive Technology (GATE) to ensure access to high-quality affordable assistive products worldwide [2]. In the last twenty-five years, progress in this sector has been praiseworthy. GATE has shown a great contribution to creating a supportive environment for disabled people. However, there is still a need for the advancement and use of rehabilitation and assistive technologies. Eyes can play a major contribution in the development of rehabilitation Engineering. Most of the physically disabled people can move their eyes only [3]. The development of eye movement-based technological devices can assist them directly[4]-[8].

The eyes are one of the most remarkable organs of human beings. Eyes contribute significantly to the perception of the world. Taking care of the eyes and addressing any vision issues promptly is essential for maintaining quality of life. The activity of various cells and structures within the eye produces biopotential through electrical signals. These electrical signals are essential for transmitting visual information from the retina to the brain. An electrooculogram, often abbreviated as EOG, is a diagnostic tool used in medical and scientific research to measure and record the electrical activity generated by the movements of a person's eyes. This non-invasive technique is valuable in understanding and analyzing eye movements, which can provide insights into various neurological and ophthalmological conditions. By monitoring the electrical potentials generated by the eye muscles, an EOG can help in diagnosing disorders such as nystagmus, strabismus, and other eye movement abnormalities. Additionally, EOGs have applications in the field of human-computer interaction, where they are used to control devices or interfaces through eye movements, making them a versatile tool with both clinical and technological significance. EOG can be utilized in automated cars to detect stress or drowsiness of the driver. Point-of-care (POC) systems can play an important role in the timely and accurate diagnosis, management, and treatment of eye conditions. Including EOG analysis in POCs has the potential to improve patient outcomes, increase access to eye care services, and enhance the overall efficiency of eye care delivery, making them an important component of modern healthcare systems. Modern technologies require fast, low-cost, and compact hardware devices that provide quick solutions to the user. These issuses can be addressed with a re-configurable approach, Field Programmable Gate Array (FPGA). In this thesis, hardware-software cosimulation is opted for as it verifies that hardware and software function correctly together. It helps to verify the functionality before building the final hardware. Therefore, this thesis aims to design EOG signal processor for detecting eye movements in FPGA. Subsection 1.1.1 describes EOG, EOG acquisition techniques, and various eye movement characteristics. It is also important to give an insight into FPGA, which is described later on in subsection 1.1.2. A brief description of the FPGA modules and the design tool are given in 1.1.3 and 1.1.4 respectively.

1.1.1 Electrooculogram

The eye can be considered as a dipole having its positive and negative poles at the cornea and retina respectively [9]. The eye has a steady corneo-retinal potential generated within the eyeball by the metabolically active retinal epithelium. The potential can be measured by placing electrodes on the skin surface around the eyes which is referred to as the electrooculography technique. This technique provides electrooculogram (EOG) which represents the recording of eye movements. The major advantages of EOG are that it is non-invasive and inexpensive [10]. Generally, the amplitude of EOG signals is in the 50 to 3500 μV range[11]. The frequency of EOG signals can vary in the range of DC to 100 Hz [12]. However, useful EOG information can be extracted from the 0 to 30 Hz range or 0 to 40 Hz range [11,13]. These values can vary with the luminous intensity [13]. EOG contains some impulsive noises such as powerline interference, and baseline drift. Therefore, filters are used for canceling these noises in the preprocessing stage. The denoised EOG signals are then ready to be processed further to the application stage. EOG signals covers a broad area of applications and research. A classification of research on EOG is shown in Fig. 1.1. Research on EOG deals with classifying eye movements, eye angle, sleep state, predicting emotion, and developing wheelchairs, game exercises [14]. The research of EOG based eye movement detection is directly connected to various disease detections. For example, normal and abnormal eye movements play an important role in detecting neurodegenerative diseases [15], diagnosing attention deficit hyperactivity disorder [16] etc. Besides, eye movements help in the communication of disabled people translating their thoughts into words [17]. On the other hand, sleep disorder threatens the quality of health of people all around the globe. Sleep stage information from EOG can be utilized to solve this disease [18]. Classification of EOG is a major concern for the future development of multimode controllers, communication devices, and HCI [19]. Most of the work done for classifying EOG is based on software [20, 14]. However, the hardware implementation for providing compact and mobile solutions for disabled persons is also getting popular day by day [21, 22]. Therefore optimized hardware implementation of EOG is still an issue of research. EOG can be implemented at the hardware level using

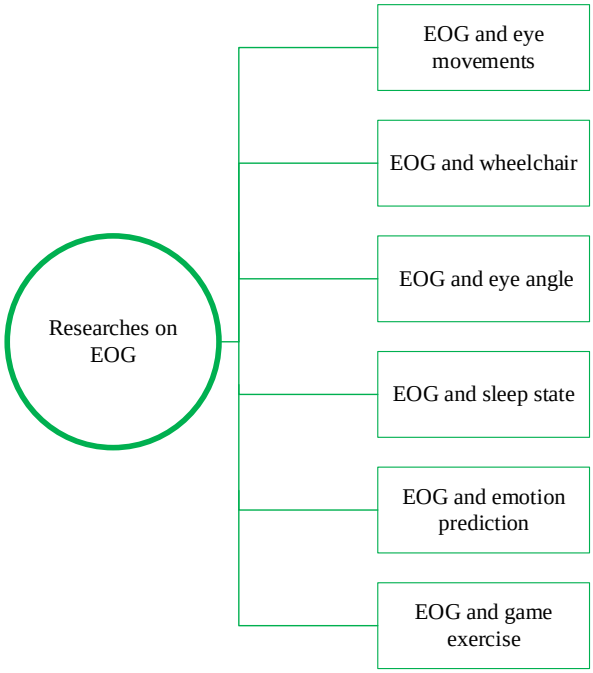


Fig. 1.1 Classification of researches on EOG

discrte circuits, micro-controllers, Arduino, as well as reconfigurable devices like FPGA.

EOG Data Acquisition Methods

EOG data can be obtained by placing electrodes near the eyes. Generally, EOG data acquisition can be categorized into main two types: dual channel and single channel acquisition.

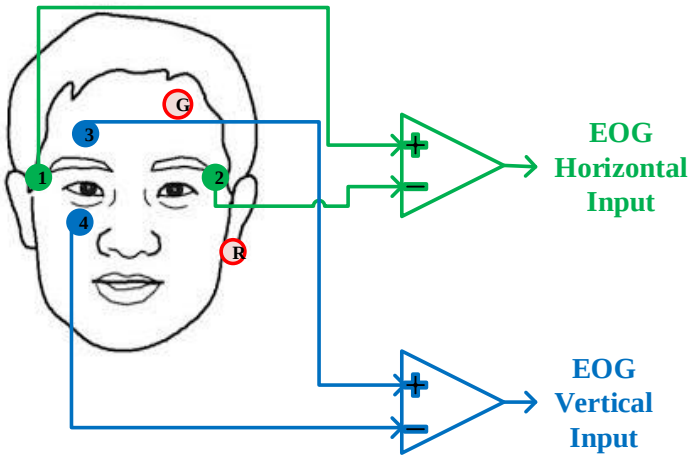


Fig. 1.2 A typical dual channel data acquisition of EOG signals

1. Dual Channel

   Dual channel EOG signals acquisition needs two pairs of electrodes. These electrodes are sensors to record the electrical activity from the eyes during eye movements. Here, two electrodes are placed on the horizontal sides of the eyes as shown by electrodes 1 and 2 in Fig. 1.2 and two electrodes i.e. electrodes 3 and 4 are placed above and under the right eye. The ground electrode, G is generally placed on the forehead and The reference electrode, R can be placed on the mastoid behind the left ear. The placement of reference electrodes can vary in individual works. Fig. 1.2 shows a dual channel electrode configuration. EOG signals contain horizontal and vertical components. The output from the electrodes provides the horizontal EOG signals, EOG_h and vertical EOG signals, EOG_v as given in equation 1.1 and equation 1.2 respectively.

$$EOG_h(t) = V_1(t) - V_2(t) \tag{1.1}$$

$$EOG_v(t) = V_3(t) - V_4(t) \tag{1.2}$$

   Here, $V_x(t)$ denotes the EOG potential recorded using electrode x where, $x = 1, 2, 3, 4$.

2. Single Channel

   Single channel EOG signals acquisition needs only one pair of electrodes. Horizontal EOG signals, EOG_h can be obtained by placing electrodes on two sides of the eyes as shown (green) in Fig. 1.2. On the other hand, the electrode pair placed above and under the eye as shown (blue) in Fig. 1.2 provides the single channel vertical EOG signals, EOG_v.

In addition to the main two EOG data acquisition techniques, there are some other techniques in the literature. Those include modified elctrode configuartion [23], eyeglasses [24], EOG sensors [25], optical sensors [26], contact lenses [27]. In this work, dual channel EOG data containing horizontal EOG signals and vertical EOG signals is used.

Eye movements

EOG provides the signal extracted from the electrode placed around the eyes. It reflects the movement of the eyes. Eye movements can be mainly categorized into three types: saccade, blink, and fixation.

1. Saccade

   Saccades can be represented as the movement of the eyes while viewing a visual scene. During this activity, simultaneous movement of both eyes is seen. Saccade duration ranges from 300 to 400 ms [28]. During this period the eyes abruptly change the point of fixation. Saccades play an important role in reading. They allow the eyes to move from one word and one line to the next. Saccades can be detected using eye-tracking technologies [24]

2. Blink

   Blinking can be defined as an automatic process of eyes getting open and closed. This is a rapid and repetitive movement of the eyelids. Eyebillinks are an integral part of the normal function of the eyes. This movement helps to spread a thin layer of tear film across the surface of the eye and ensures the moisture in eyes. Blinks also protect eyes from damage caused by excessive brightness by reducing the amount of light entering the eye. Generally, blinking occurs throughout the whole day. The average blink duration ranges from 100 to 400 ms [9]. The average blink rate can be 12 to 19 blinks per minute at rest. This rate can be influenced by environmental and physical factors. Environmental factors include temperature, relative humidity, and brightness. The physical factors include the health of the eyes, activity level, level of cognitive workload, or fatigue.

3. Fixation

   Fixation is the stationary state of the eyes. Fixations represent the interval between two saccades. Fixation time is the time to focus after stopping the eyeball which ranges from 100 to 200 ms [9]. This movement helps to construct a continuous and coherent visual perception. For example, during reading, fixations occur at each word in a text and process the visual information within each word.

In the literature, a good amount of work has been done with blink detection, classification of saccade and blink. In addition, to blink information, EOG signals can provide information on various eye movements such as: up, down, right, and left. These eye movements can be easily detected using EOG signals as the signals represent significant differences for different eye movements. Literary works show evidence that EOG signal processing for eye movement classification is getting more popular for human machine interfaces (HMIs). In this work, EOG is processed for blink detection, and eye movement classification that can further be used in other HMI applications.

1.1.2 Reconfigurable Computation Architecture- FPGA

Digital hardware systems can be implemented in various devices such as Field Programmable Gate Array (FPGA), Complex Programmable Logic Device (CPLD), Simple Programmable Logic Device (SPLD), microcontroller, and others.
In this work, FPGA is utilized to implement the designs at the hardware level because of its characteristics. FPGA refers to a type of integrated circuit that can be reconfigured or programmed after manufacturing to perform various digital logic functions. The reconfigurable architecture makes FPGA highly adaptable for various tasks. FPGAs are capable of parallel processing, which means they can perform multiple tasks simultaneously. This makes them suitable for tasks like signal processing, and real-time data analysis [29]. FPGAs have low latency and high throughput, making them suitable for applications that require fast data processing. FPGAs are valuable in the development and prototyping phases of electronic designs. FPGAs help in quick testing and iterating designs before committing to application specific integrated circuits (ASICs) or other fixed hardware. This custom-made circuit designing scheme ensures dynamic resource utilization to speed up data processing- the hardware acceleration. FPGAs are energy efficient, especially when compared to power-hungry Graphics Processing Units (GPUs). Because FPGAs execute tasks in hardware, they can often perform the same calculations with significantly lower power consumption. FPGAs also offer longer lifespans compared to off-the-shelf GPUs. Therefore, it can be said that FPGAs are a suitable choice when it is needed to ensure hardware customization,

low latency, and specialized acceleration for specific tasks.

Based on the advantages of FPGA, it can be useful in proof-of-concept designs. This kind of design helps to demonstrate whether an idea can be turned into a reality. Therefore, in this work, FPGA is chosen for developing the designs.

FPGAs are typically programmed using Hardware Description Languages (HDLs) like Very High-Speed Integrated Circuit Hardware Description Language (VHDL) or Verilog. There are also higher-level programming tools and languages that make FPGA development more accessible. Before programming FPGA, it is needed to get insights into the basic structure of FPGA and its components.

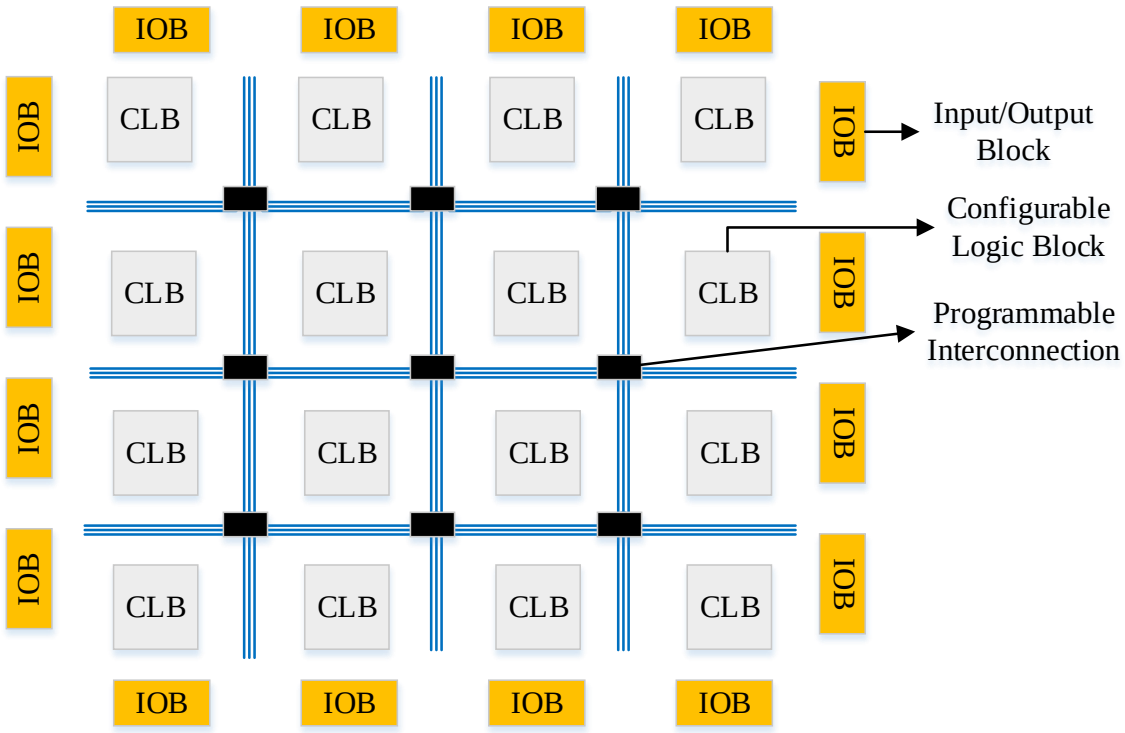


Fig. 1.3 Basic structure of an FPGA chip

Figure 1.3 shows a typical internal structure of an FPGA chip. Generally, an FPGA consists of three basic components. They are:

1. Configurable Logic Blocks (CLB)- responsible for implementing the core logic functions.

2. Programmable Interconnection – responsible for connecting the Logic Blocks.

3. Input/Output Blocks (IOB) – connected to the Logic Blocks through the routing and make external connections.

The logic functions of these blocks and the connections are given by the designer as needed. The CLB is the fundamental block in FPGA that contains flip-flops (FFs), look-up tables (LUTs), and multiplexers inside. FF refers to a binary register circuit that can store one bit. A flip-flop is the smallest storage resource on the FPGA. It can save logic states between clock cycles on an FPGA circuit. LUT represents a collection of gates hardwired on the FPGA. It can store a predefined list of outputs for every combination of inputs. LUTs provide a fast way to retrieve the output of a logic operation because possible results are stored and then referenced rather than calculated. A multiplexer represents a circuit that can select between two or more inputs and then return the selected input. There can be some other blocks such as memories (BRAMs, LUTRAMs, ROMs, shift registers), Digital Signal Processors (DSP), Phase-Locked Loop (PLL) clock generators, etc. in a modern FPGA.

1.1.3 Module Selection

This thesis aims to implement EOG signals processor at the hardware level. Hardware based digital and embedded systems are becoming more popular due to their multifunction capability, low cost, and high-performance accuracy. FPGA has been chosen for this study as it is simple and easy to design as well as has the advantage of reprogrammable functionality. FPGA contains more logic blocks than CPLD or SPLD. It allows greater customization and more complex processes than CPLD and SPLD. Also, microcontroller provides reprogramming of firmware but FPGA has the advantage of changing the functionality of both hardware and firmware. FPGA has the advantage of hardware acceleration as it can be used to accelerate workloads and gain significant benefits. Parallel computing is another advantage of the FPGA which allows to handle multiple workloads. This provides the scope to work on different stages of tasks concurrently which cannot be done with GPUs. Some other advantages of FPGA are smaller board space, power efficiency, and reliability. Therefore, in this thesis, two FPGA modules: Zedboard Zynq-7000, and Zynq Ultrascale+ are chosen to implement the

designed works. A short description of the selected modules is given below.

Zedboard Zynq-7000

ZedBoard is a low-cost development board manufactured by Digilent. This board employs Xilinx Artix-7 FPGAs coupled with a dual-core ARM Cortex-A9 processor [30]. The ZedBoard has a broad range of applications, such as digital signal processing (DSP), image processing, industrial automation, etc. This FPGA system-on-a-chip (SoC) based board enables the designers to accelerate the custom DSP algorithm, as it is possible to program Zedboard whenever necessary [31]. The first design of this thesis uses ZedBoard for hardware implementation.

Zynq UltraScale+

The ZCU106 Evaluation Kit contains a Zynq™ UltraScale+™ MPSoC EV device and supports all major peripherals and interfaces, enabling development for a wide range of applications [32]. This kit is able to make designs for video conferencing, surveillance, Advanced Driver Assisted Systems (ADAS), streaming, and encoding applications. The included ZU7EV device is equipped with a quad-core Arm® Cortex®-A53 applications processor and a dual-core Cortex-R5 real-time processor. The second design of this thesis uses Zynq UltraScale+.
Appendix D provides a detailed description of the above-mentioned modules.

1.1.4 Design Tool Selection

The goal of this thesis includes hardware-software codesigning of the EOG signal processors. Hardware-software codesign refers to the concurrent designs of hardware and software components of complex electronic systems. These designs are capable of merging hardware and software that can ensure optimization, and satisfaction of the design constraints such as cost, performance, and power consumption. These types of designs can be very beneficial for real-life problems dealing with a pragmatic approach. The pragmatic approach checks the practical feasibility of a defined task. Therefore, the designs of this work use hardware-software codesign. For this design purpose, proper tool selection is necessary.
In this thesis, the Xilinx system generator (XSG) is selected for design at the hard-

ware level. XSG is a design tool for the implementation of DSP algorithms in Xilinx devices. It is a MATLAB Simulink add-on that enables the development of architecture-level FPGA designs using graphical block programming. Xilinx FPGAs platforms contain Block RAMs, DSP Slices, PCI Express support, and programmable fabric, etc. It is possible to process in both parallel and pipelining approaches as all of these compute resources can be used simultaneously. In XSG hardware description language is used to assemble FPGA building blocks into a circuit. This design is easier compared to typical high-level languages. The two most popular hardware description languages are VHDL and Verilog. In XSG the system is designed in Matlab Simulink and then synthesized the design into an FPGA. High-level synthesis (HLS) uses a high-level programming language like C, and C++ to describe the functionality of a digital circuit or electronic system. HLS tools then automatically convert this high-level description into a register-transfer level (RTL) hardware description, which can be implemented on programmable hardware such as FPGAs or ASICs. HLS helps in building and verifying hardware. Therefore, optimization of the hardware design is possible. The designer can design at a higher level of abstraction and the tool can complete the RTL implementation.

The design flow of FPGA implementation in Xilinx system generator is given in Figure 1.4. In Software co-simulation, all Xilinx blocks are connected between two blocks - Gateway In and Gateway Out, which behave as input and output respectively for the hardware design. The Xilinx blocks work with fixed point format, therefore, it is necessary to convert real-world signals of floating format into the fixed point and vice versa. In this case, Gateway In and Gateway Out blocks act as translators for format conversion.

After software simulation, the System Generator token needs to be configured to allow the model to be compiled into hardware. The XSG token dialog box needs to be configured with adequate settings for compilation, synthesis, and clocking. At first, the compilation Target is chosen by specifying the FPGA platform. After that, the synthesis tool is involved in synthesizing the design. It includes setting some parameters such as hardware language, clock etc. After the configuration, a bit stream (.bit) file is generated. Then, the hardware co-simulation target is se-

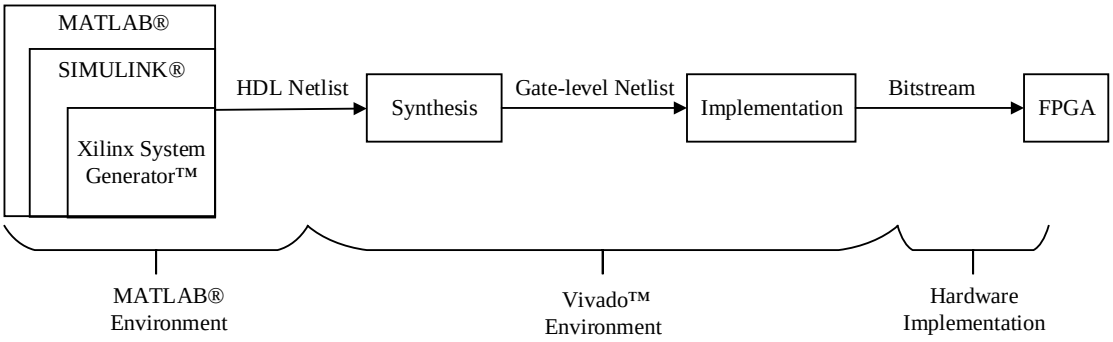


Fig. 1.4 Design flow of FPGA implementation using XSG

lected and a block will be generated. This block can be then added to the design and all the blocks for both software and hardware can considered to be co-exist. In this work, firstly ZedBoard is chosen to implement the binary classification. Then, Zynq Ultrascale+ is chosen to implement the multiclass classification. Both modules are designed using XSG.

1.2 Present State of the Problem

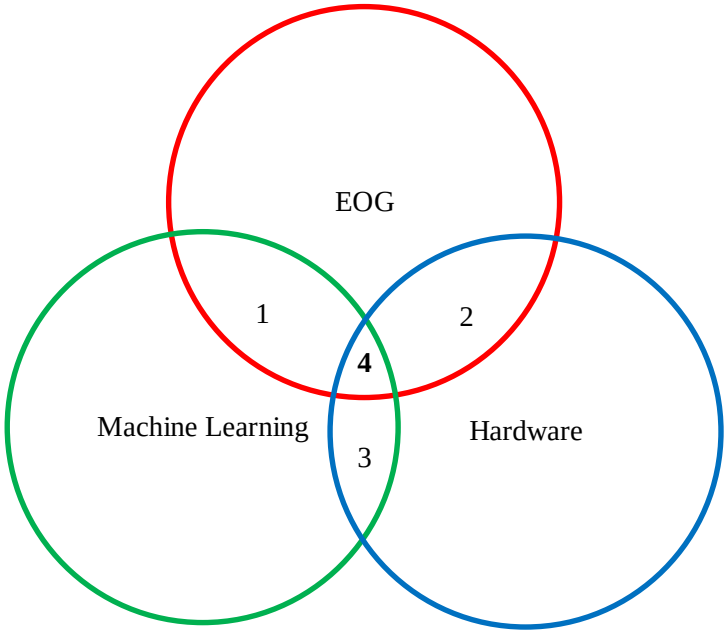


Fig. 1.5 A ven diagram illustrating the present state of the problem

In this section, the present state of the problem for EOG hardware implementations is depicted. The world is heading towards point-of-care testing systems.

Blinks and eye movements detected from the EOG signal are utilized to determine various eye conditions. EOG signals are being studied through machine learning for various eye condition analyses and disease detection which is indicated by the "area 1" in Fig. 1.5. There are some works of EOG that include hardware implementations as indicated by "area 2". There are studies that include hardware implementation without using machine learning as given in "area 3". However, as machine learning is getting more popular day by day, more focus on the combination of machine learning & re-configurable hardware implementation of EOG signals is more demanding nowadays. A common platform of machine learning, EOG hardware implemented works are indicated in "area 4". These can be utilized for digital point-of-care systems. These type of implementations includes the design and implementation of various stages: preprocessing, feature extraction, and classification. Efficient designs need optimization throughout each stage. Therefore, the need for compact and optimized hardware-based systems for eye movement detection arises to overcome this issue. This thesis addresses the issue by providing proof-of-concept complete digital systems for blink and various eye movement detection.

1.3 Specific Objectives

Eye movement is a frequent physiological activity of human beings. It possible to collect information on these eye movements by processing EOG signals . An efficient algorithm to process EOG is important to integrate it into point-of-care devices and human machine interfaces (HMIs) applications. It is also important to choose a suitable platform to implement the algorithmic design. Therefore, hardware-software codesign can be the proper solution to verify the EOG signal processing algorithm. However, these algorithm needs to be hardware-friendly i.e. the algorithms must be designed in a way to use few resource blocks, consume low power, and offer low time delay.

Field Programmable Gate Array (FPGA) can be a suitable platform to implement digital signal processing algorithms because of its characteristics: low cost, low power consumption, re-configurable architecture, small size, and high speed.

This work aims to codesign hardware-software multichannel FPGA-based complete EOG processors adopting a machine learning approach. The designed processors detect eye blinks and various eye movements. The implemented stage includes: preprocessing, feature extracting, and classifying.
The specific objectives of this thesis are as follows:

1. To develop hardware-friendly algorithms to classify the EOG signals.

2. To design compact systems of EOG processors on FPGA using the developed algorithms.

1.4 Contribution of the Work

EOG signals provide insights into eye movement patterns. Many existing works of EOG deal with eye movement detections, and eye conditions and disease detections based on the the detected eye movements. This thesis provides the first systematic review of EOG hardware implementations to provide an idea on exisiting reasearch opportunities. Digital systems of EOG signals can be helpful for classifying blinks and eye movements. This thesis provides hardware-software codesign of the blink detector and the eye movement classifier using EOG signals. Blink detectors can be readily integrated with human machine interfaces. The eye movement detector can pave the way for eye e-health as this system will open the door for other diseases to be detected from eye movements.

1.5 Thesis Outline

The thesis presents the design of the software backend and the hardware frontend of systems dedicated to electrooculogram (EOG) signal processing. The EOG signal processors are designed as binary classifier for blink detection and mutliclass classifier for detecting six different eye movements. The overall thesis organization is depicted in Fig. 1.6. This thesis contains a total of six chapters. A brief description of these chapters is given below.
Chapter 1 describes the background of the EOG signal first. After that, the method of EOG signal acquisition, and basic eye movements are explained. The problem

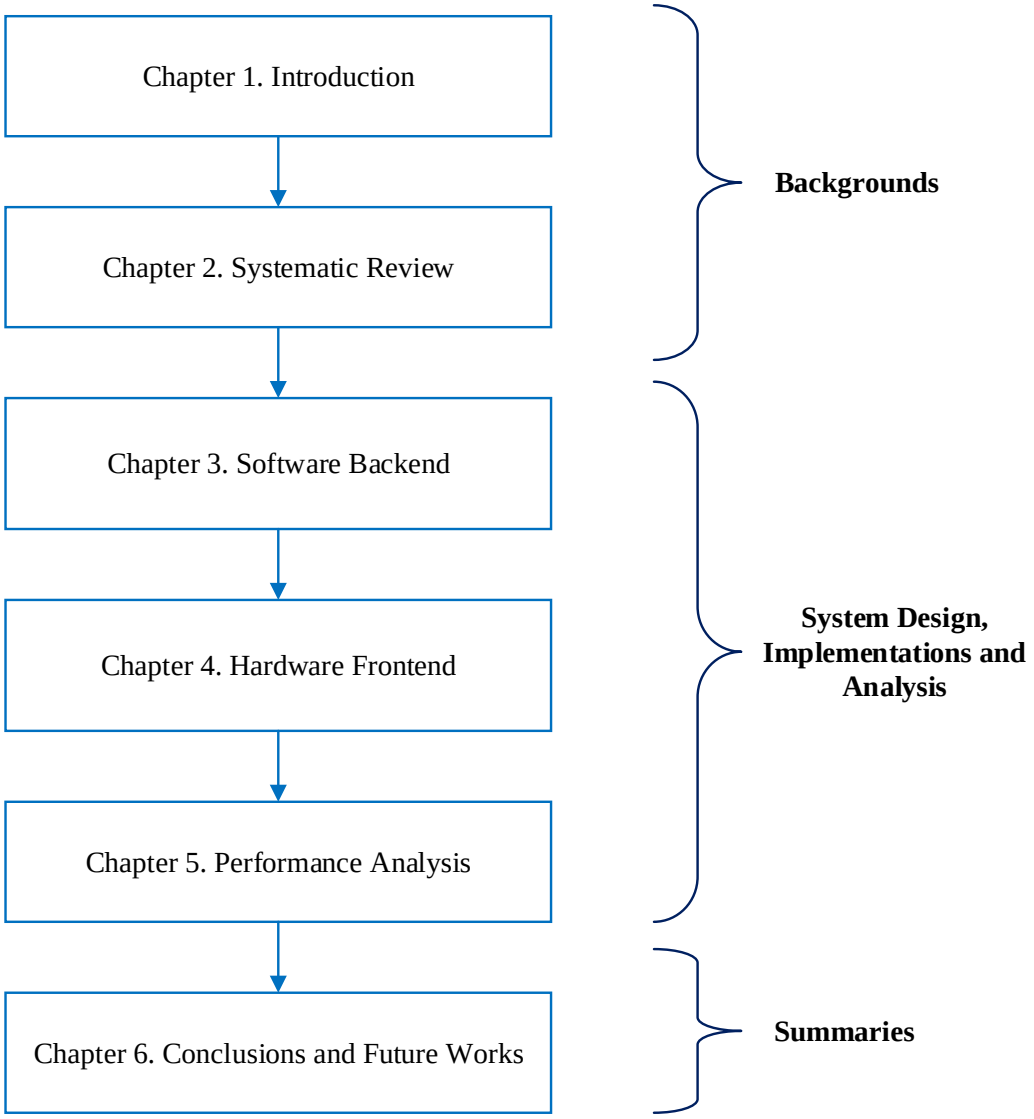


Fig. 1.6 Structure of the thesis

statement and significance of the study are also discussed.

Chapter 2 reviews the application of EOG signals in various sectors. The previous works on EOG signals are discussed. A systematic review is presented on EOG hardware implementations. The systematic review is focused on providing a structured discussion on solely EOG based point of care systems.

Chapter 3 shows the software backend for the design of the EOG binary classifier for blink detection and the EOG multiclass classifier for six eye movements detection.

Chapter 4 shows the hardware frontend design of the EOG binary classifier for blink detection and the EOG multiclass classifier for six eye movements detec-

tion. It shows the FPGA implementation approach. The system architecture of hardware design of various subsystems in Xilinx system generator are explained Chapter 5 represents the performance analysis of the designed processors. It includes both software and hardware performance and checks their agreements. Resource utilization and power consumption analysis are given in this chapter. The comparative study with previous works is also presented.

Finally, Chapter 6 presents the conclusions of the thesis and summarizes the overall contribution of this research. Some scopes of possible future works are also mentioned at the end.

Chapter 2: Systematic Review

The eyes can be a great tool to assist disabled people with technological devices run by eye movements. The hardware-implemented platform increases feasibility in this area. Eye diseases are one of the major contributors to disabling conditions. Negligence in regular checkups is the key reason for deteriorating eyesight. The high cost of checkups for disease detection is another reason for not regularly receiving health check-ups. Consequently, these diseases ultimately turn severe and can take severe form, leading to blindness. A preventive health checkup can prevent the disease from worsening and save many people from losing their working ability. Around 2 billion people face vision impairment and various ocular diseases worldwide. Efficient hardware can provide quick decisions for emergency medical services, remote medical care, and intensive care. The goal of providing emergency and fast services can be achieved through point-of-care (POC) systems. In this chapter, at first, some real-life applications of electrooculogram are outlined. Then, the advantages of the POC systems are outlined. A systematic review approach is employed to review the state-of-the-art works on EOG hardware systems. A systematic review is a rigorous and comprehensive method of summarizing and synthesizing existing research evidence on a specific research question or topic. This chapter includes the method and findings of the review.

2.1 Electrooculogram Applications in Real-Life

The eyes are an integral part of the human body. It helps disabled people to communicate with the external world by using eye movements [5]-[8]. The assistive devices developed based on eye movements are great tools to ease their life. Additionally, eye diseases also contribute to creating disabling conditions. There are various diseases such as nystagmus, ocular dysfunction, and dry eyes that can be detected just by using Electrooculogram (EOG) signals [33]-[37]. These diseases primarily cause blurriness. In the long run, they can cause blindness

leading to vision disability. Efficient hardware can provide quick decisions for eye movement detections. Thus, hardware-implemented platforms are necessary to be developed for both rehabilitation purposes and point-of-care systems.

2.2 Electrooculogram Point-of-care Systems

Point-of-Care (POC) means the point in time when healthcare services and products are being provided to patients at the time of care [38]. POC systems are important as they provide some advantages such as early screening leading to early diagnosis, separating inpatients & out-patients, critical & non-critical patients, monitoring recovery, and finally providing early recovery to immunity. Some examples of POC systems are home pregnancy tests, blood glucose monitors, and urine dipsticks etc. Fig. 2.1 outlines the importance of the POC testing

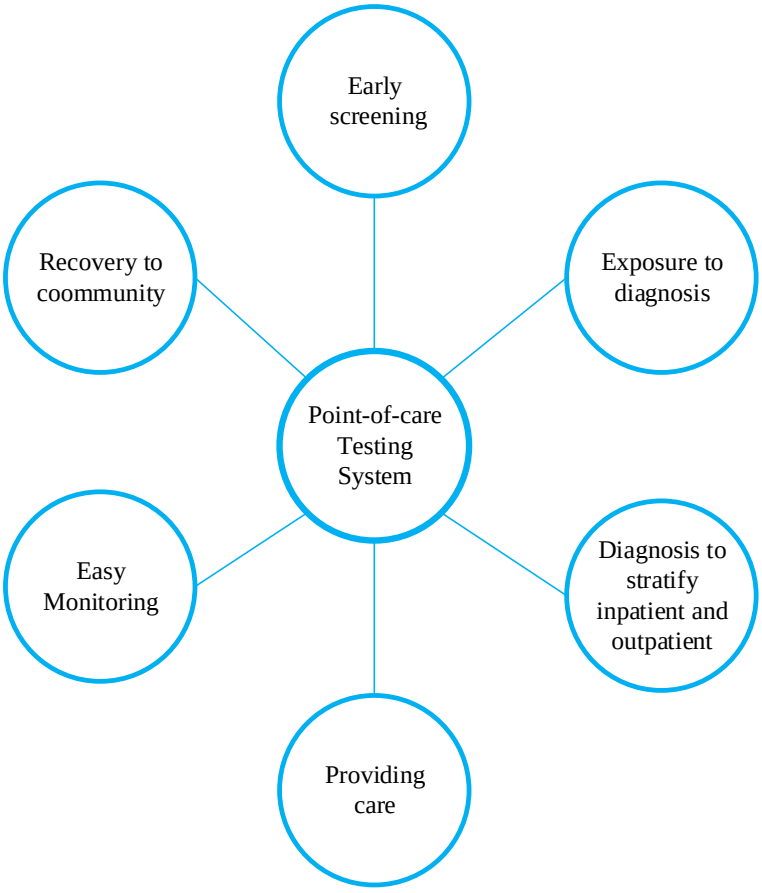


Fig. 2.1 Importance of point-of-care testing system

system. Obtaining signals from eyes by electrooculography and implementing

them at the hardware level can pave the way for POC systems for various eye conditions detection.

2.3 Methodology of Systematic Review

In this study, a systematic review process [39] to find the research trend and the state of the art of EOG hardare implementations to develop EOG point of care (POC) systems. The review is conducted following the Preferred Reporting Items for Systematic Reviews and Meta-Analyses (PRISMA) protocol and the Problem, Intervention, Comparison, and Outcomes (PICO) statement [40, 41]. The PRISMA flow diagram and the number of publications of each stage are shown in Fig. 2.2. The focus is given to the works solely based on EOG excluding hybrid works of EOG. The search string includes classification and hardware as EOG point of care systems use hardware applications based on classification. Studies containing hybrid works of EOG and any other signal, non-human subjects (e.g., animals), and non-English papers are excluded.

The review process is done mainly in two phases: primary and secondary phases as shown in Fig. 2.2. These phases are described below.

2.3.1 Primary Phase

In the primary phase, identification and screening of the research articles are done.

1. Identification

   This stage involves investigating related studies based on the search string in selected databases. The papers are extracted from major science-related databases, namely ScienceDirect, Springer Link, IEEE Xplore, PubMed, and Google Scholar.

   The search string used is defined as: (EOG AND Classification AND (FPGA

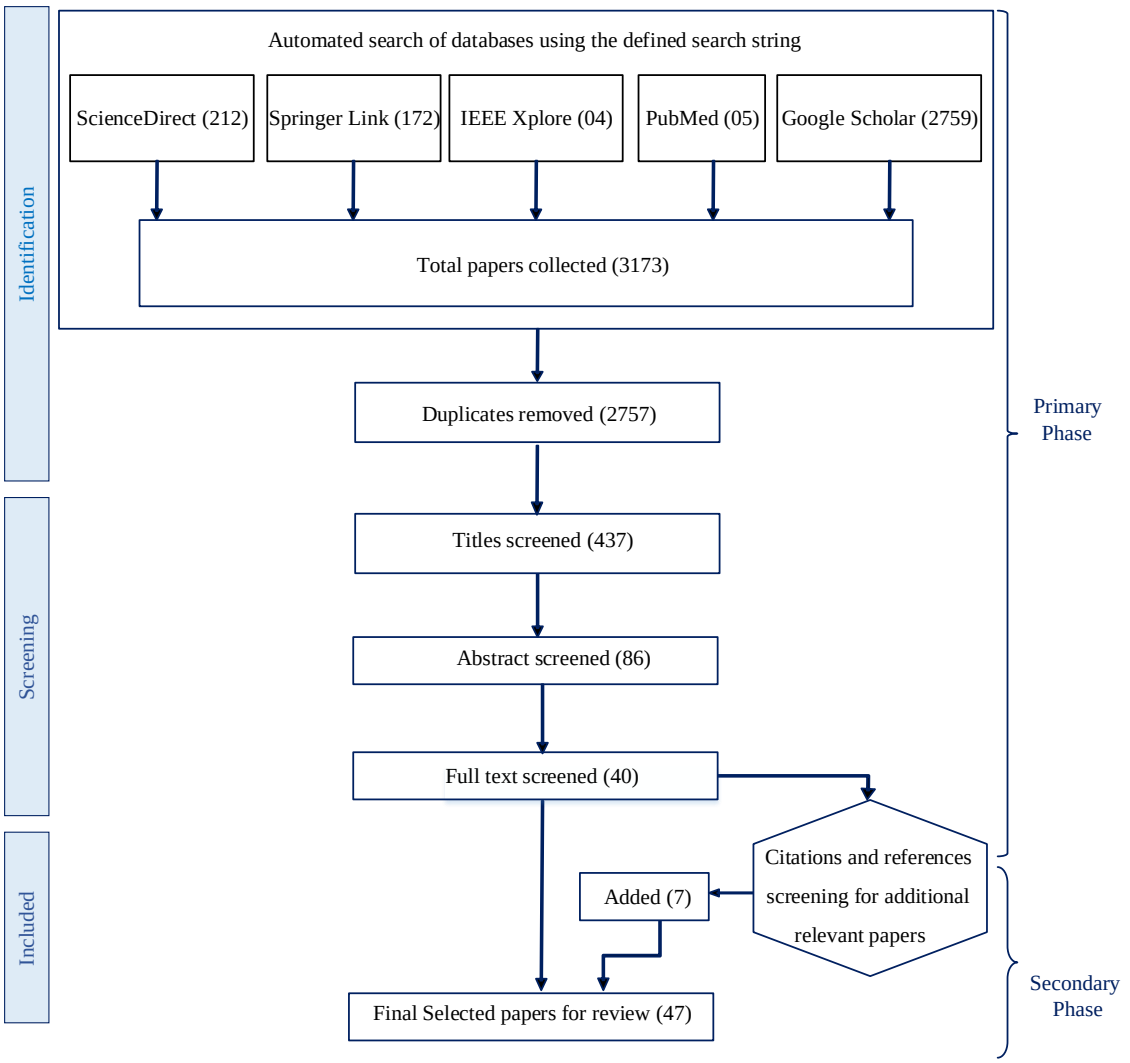


Fig. 2.2 PRISMA flow diagram for the initial study selection of the systematic review

OR Hardware) NOT Hybrid).

The searches have been done between the 5th–15th of May 2023 and covered publications in the range of 2018–2023. Selected papers are written in English and from conferences and journals. A total of 3173 papers have been collected from this search. Then, the duplicates are removed using the EndNote tool. Then, 2757 papers were used for screening in the next stage.

2. Screening

The screening depends on the titles and abstracts in the database. Duplicate articles have been first removed and further screening is carried out on the remaining selected papers. Articles have been excluded if 1) have hy-

bridization of EOG with any other signal, and 2) have no information about the hardware implementations. EndNote tool is used to analyze and screen the papers. To qualify the conformity and correspondence, the abstract-screened articles are then subjectively screened by authors. After the full-text screening, 40 papers have been selected.

2.3.2 Secondary Phase

Sanka and Cheung [42] recommended a combination of both the automated search and a manual search in systematic reviews. Therefore, in the secondary phase, the references and citations of the 40 selected papers of the primary phase are checked. After screenings, 7 more relevant papers are added to the initial 40 selected papers. Finally, a total of 47 papers are included for the review.

2.3.3 Research Findings

51% of the studies are journal papers and the rest 49% are conference papers. EOG studies cover classifying eye movement, eye angle, sleep state, predicting emotion, and developing wheelchairs, and game exercises as mentioned in section 2.1. At first, the studies are categorized based on the data acquisition techniques: dual channel, single channel, and others. Then, based on the detection or classification techniques can be categorized in the studies: classical detection approach and machine learning approaches. Then, hardware implementations are categorized based on the hardware used as reconfigurable (FPGA) and non-configurable. These categories are briefly described in the subsequent sections.
Among the selected papers, 59% of works study with dual channel data while 29% on single channel. Also, 12% of them worked on other types of data acquisition which includes Eyeglasses [24], EOG sensors [25], Biosensors [43], Optical sensors [26], Capacitive sensing [44], Smart glasses with EOG sensors [45], Magnet[46]. Modified single channel has used two electrodes in a little bit of changed position [23]. Table 2.1 shows the summary of the EOG acquisition process.

Table 2.1: A summary of EOG acquisition process

Method	References
Dual Channel	Rotariu et al. [10], Das et al. [11], Asanza et al. [13], Fernandez et al. [15], Latifoglu et al. [16], Kishore Kumar and Narayanam [20], Chowdhury et al. [21], Borkar et al. [22], Hou and Smitha [47], Shivaprasad and Vishwanath [48], Kabir et al. [49], Golparvar and Yapici [50], Abdel-Samei et al. [51], Archana et al. [52], Lin et al. [53], Parra et al. [54], Gundugonti and Narayanam (2021) [55], Anuradha et al. [56], Zou and Zhang [57], Hossieny et al. [58], Lopez et al. (2018)[59], and Martínez-Cerveró et al. [60]
Single Channel (Horizontal)	Zaeni et al. [19], Daou et al. [43], Archana et al. [52], Fan et al. [61], Simoes et al. [62], Prabha et al. [63], Lopez et al. (2019) [64], Bastes et al. [65]
Single Channel (Vertical)	Molina-Cantero et al. [17], and Hayawi and Waleed [66]
Others	Savastaer and Tepe [23] (Modified), Ryu et al. [24] (Eyeglasses), Pai et al. [25] (EOG sensors), Masai et al. [26] (Optical sensors), Li et al. (2022)[27] (Contact lens), Daou et al. [43] (Biosensors), Matthies et al. [44] (Capacitive sensing), Li et al. (2020) [45](Smart glasses), and Almansouri et al. [46] (Magnet)

2.4 Detection Approaches

After data acquisition, the data needs to be preprocessed for denoising the EOG signal. The unwanted noises such as baseline wander, and 50/60 Hz power line interference needs to be eliminated in this stage. Then the data is processed further for classification. EOG classifications or detection approaches are found mainly in two categories:- classical detection approaches and machine learning approaches.

Classical detection approaches need preprocessing and suitable movement algorithm as shown in Fig. 2.3 (Red box). A basic block diagram of EOG processing using machine learning and deep learning is shown in Fig. 2.3 (Blue box). The raw EOG data must go through preprocessing, feature extraction and classification stages.

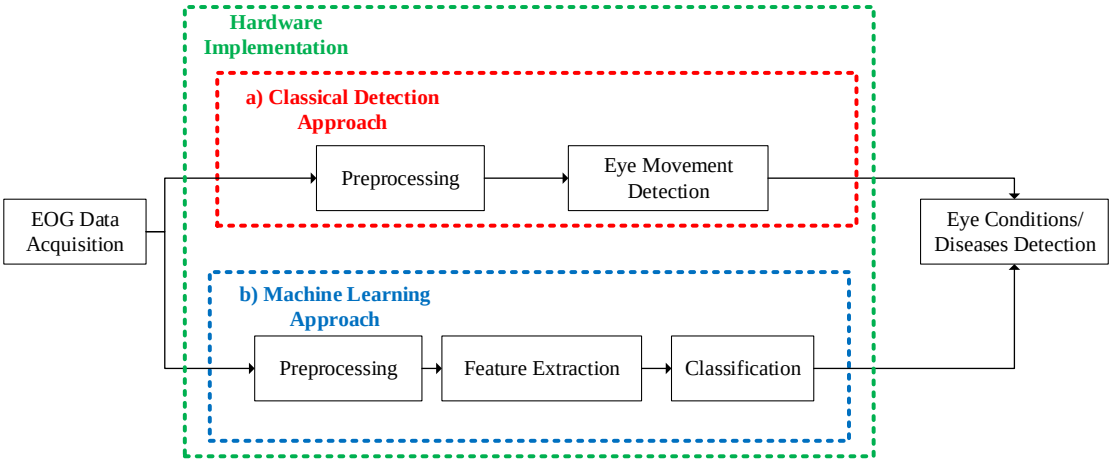


Fig. 2.3 Hardware implementation of EOG processor

In literature, 42% of the works are found to adopt classical detection approaches whereas the rest 58% adopt machine learning approaches. It indicates the recent trend of EOG signal processing with machine learning approaches.

2.5 Hardware Implementations of EOG

The implementation level of the selected studies has been categorized into two: FPGA and discrete circuits or micro-controllers.

More than three-fourths (26%) of the works were implemented on FPGA which involves the process of determining the physical resources of FPGA and utilizing them. The rest of the works (74%) were implemented on discrete circuits or microcontrollers as shown in Fig. 2.4.

It is complex to implement systems efficiently on FPGA as it requires some expertise. Despite the tendency of FPGA to consume more power than a microcontroller or an ASIC, FPGA requires a smaller board space and shows energy efficiency than the equivalent discrete circuit. FPGA based implementations also provide some benefits over others as they provide the flexibility of reconfiguring the design.

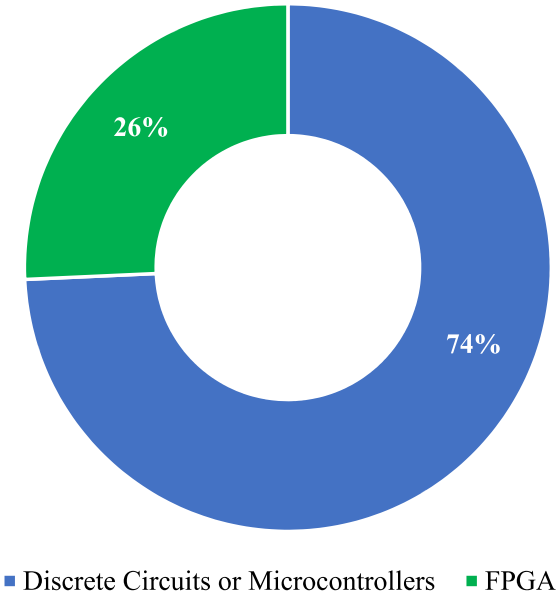


Fig. 2.4 Ratio of EOG signal implementations in different hardware.

2.5.1 FPGA based EOG Implementations

Cano et al. [67] developed an efficient design a convolutional neural network and implemented it on FPGA device. Fernandez et al. [15] designed a FPGA based system for the generation of multiple visual stimulus signals and for EOG acquisition. Kumar and narayanam (2020a) [68] developed a denoising filter with differential evaluation (DE) algorithm with fewer sign power of two which was verified using Altera DSP Builder. Kumar et al. [69] proposed a modified FIR filter using Canonical signed digit (CSD) and Kumar and Narayanam (2020b) [70] proposed a modified FIR filter using canonical signed digit representation and compressor techniques for denoising the EOG signal. In both works, the proposed models were implemented and verified on FPGA. Gundugonti and Narayanam (2021) [55]]developed an architecture of the discrete Haar wavelet transform which was synthesized using Cadence RTL compiler. Kishore Kumar and Narayanam [20] detected the saccades and blinks. They denoised the EOG signals with transposed direct form FIR filter. The Haar wavelet transform was

used for decomposition of denoised EOG signal. The modified eye movement detection algorithm was synthesized on FPGA. Gundugonti and Narayanam (2022) [71] proposed area and power efficient FIR filter structure using common subexpression elimination (CSE) algorithm with CSD method which was later verified in Xilinx-Simulink environment. Asanza et al. [13] used preprocessing and feature extraction in software level. They developed a custom hardware architecture for EOG classification model in al FPGA card. Das et al. [11] proposed a reconfigurable preprocessing technique using FIR and IIR filters for serial processing of EOG horizontal and vertical data and implemented it in Xilinx Zynq-7000 FPGA Table 2.3 summarizes FPGA Implementation of EOG. As it is seen, preprocessing stage is currently being implemented in FPGA. It is noticeable that there is a scope for extracting the features in a reconfigurable platform. The advantages and limitations of the reconfigurable processing techniques are summarized in Table 2.3.

Das et al. [11] proposed a design to implement a fast EOG serial preprocessor using FIR and IIR filters. The Pearson Correlation Coefficient of 0.99 and a Mean Root Squared Error in the 10^{-3} range were found. The on-chip power consumption for this design was 0.271 watts. The limitation was a delay because of serial processing which was minimized by using a fast counter. Kumar and Narayanam (2020a); Kishore Kumar and Narayanam [68, 20] used a filter with differential evolution (DE) algorithm. The mian advantage of this filter was using fewer sign-power-of-two (SPT) terms to optimize the denoising filter. This hardware used less area than conventional filters. The limitation of their work was that the coefficients were best suitable for Application-specific integrated circuit (ASIC) implementations only. Kumar and Narayanam (2020b) [70] proposed FIR architecture that uses canonical signed digit-based (CSD) multipliers and 3:2 or 4:2 compressors to achieve greater improvement in power and delay compared to the conventional shift-add method of multiplication. CSD was used to reduce the multiplication's design complexity by representing the filter coefficients in

Table 2.2: A summary of FPGA implementation of EOG

References	Preprocessing	Feature Extraction	Classification or Detection	Algorithm
Cano et al. [67]	×	×	✓	CNN
Kumar and Narayanam (2020a) [68]	✓	×	×	-
Kumar and Narayanam (2020b) [70]	✓	×	×	-
Kumar et al. [69]	✓	×	×	-
Gundugonti and Narayanam (2021) [55]	×	×	✓	Haar DWT
Kishore Kumar and Narayanam[20]	✓	×	✓	Haar DWT
Gundugonti and Narayanam (2022) [71]	✓	×	×	-
Asanza et al. [13]	×	×	✓	Cubic SVM
Das et al. [11]	✓	×	×	-

Table 2.3: A summary of reconfigurable EOG preprocessing techniques

Preprocessing Techniques	**Advantages**	**Limitations**	**References**
FIR & IIR Filter (Serial Processing)	Almost half resource of traditional designs	Delay	Das et al. [11]
Filter with DE algorithm	Fewer SPT terms, less area, low power	Best suitable for ASIC implementation	Kumar and Narayanam (2020a) [68] & Kishore Kumar and Narayanam [20]
FIR filter (CSD+compressor)	Reduced delay	High area and power	Kumar and Narayanam (2020b) [70]
Filter (CSE + CSD)	Low power & area	Delay	Kumar et al. [69] & Gundugonti and Narayanam (2022) [71]
DWT	Low resource utilization	Shift sensitivity and poor directionality	Meeravali et al. [72]

CSD format. The final designed filter provided reduced delay but the area and power are higher than CSD. Kumar et al. [69], and Gundugonti and Narayanam (2022) [71] used an area and power efficient filter for real-time noise reduction of EOG using a common sub-expression elimination method. This filter architecture offered a 148.17% area increment and a 114.45% power increment over traditional filter architecture. However, the delay is higher than [70]. Meeravali et al. [72] developed an efficient wavelet-based architecture for denoising EOG signals. However, it showed shift sensitivity and poor directionality.

2.5.2 Other implementations of EOG

This section gives an overview of the non-configurable implementation of EOG processing of the selected works. Table 2.4 summarizes the implementation of discrete circuits and micro-controllers and eyewear. They have some advantages such as low time requirement for performing the operation, ease of use, simple troubleshooting and system maintenance, and flexibility due to their small size.
Microcontrollers for the data acquisition stage is prominently seen in state-of-the art literature [10,16,19,21,22,26,46,48,49,51,52,63,65]. Discrete circuits and microcontrollers are utilized for data acquisition and processing stages [23,44,50, 54]. Pai et al. [25] used a prototype with EOG sensor. Masai et al. [26] used a smartwear with sensors. Jins meme smartglasses are found to be used for data acquisition [45, 73,74].

2.6 State-of-the-Art

The EOG hardware implementations cover a large area. In this section, the performance of the state-of-the-art studies that only deal with eye movement detection is outlined. Table 2.5 summarizes the accuracy of the various techniques used in the studies.
Rotariu et al. [10] utilized dual channel EOG to develop an electronic medical de-

Table 2.4: A summary of non-configurable hardware implementations of EOG

Hardware	**Implemented stage**	**References**
Micro-controllers	Data acquisition	Rotariu et al. [10]
		Borkar et al. [22]
		Bastes et al. [65]
		Chowdhury et al. [21]
		Shivaprasad and Vishwanath [48]
		Kabir et al. [49]
		Latifoglu et al. [16]
		Zaeni et al. [19]
		Almansouri et al. [46]
		Archana et al.[52]
		Lopez et al. (2018) [59]
		Martínez-Cerveró et al. [60]
	Classification	Prabha et al. [63], Daou et al. [43]
Discrete circuits & micro-controllers	Data acquisition	Savastaer and Tepe [23]
	Data acquisition with sensors	Matthies et al. [44]
		Masai et al. [26]
	Data acquisition (Discrete circuits), Processing (μC)	Parra et al. [54]
	Data acquisition & Processing	Golparvar and Yapici [50]
		Abdel-Samei et al. [51]
Others	Data acquisition & Processing	Pai et al. [25]
		Masai et al. [26]
		Li et al. (2020) [45]
		Rostaminia et al. [73]
		Yeo at al. [74]
		Li et al. (2022) [27]

Table 2.5: A summary of present state-of-the-art EOG eye movement detection approaches

Approach	**Algorithm**	**Accuracy**	**Reference**
Classical Detection	Threshold	90%	Rotariu et al. [10]
	Threshold	-	Borkar et al. [22]
	DFT	90%	Bastes et al. [65]
	DOSbFC	94%	Ryu et al. [24]
	Threshold	89%	Hou & Smitha [47]
	Threshold	96% to 98%	Chowdhury et al. [21]
	Conditional Statement	-	Prabha et al. [63]
	Conditional Statement	83.3%	Lopez et al. (2019)[64]
	Threshold	-	Shivaprasad & Vishwanath [48]
	Threshold	Upto 97%	Savastaer & Tepe [23]
	Haar DWT	-	Kishore Kumar& Narayanam [20]
	Haar DWT	-	Gundugonti & Narayanam [55]
	Threshold	-	Parra et al. [54]
	Threshold & others	Upto 100%	Golparvar & Yapici [50]
	Conditional Statement	98%	Anuradha et al. [56]
	Conditional Statement	90%	Daou et al. [43]
	Conditional Statement	Upto 89.63%	Li et al. (2022) [27]
	Threshold	-	Abdel-Samei et al. [51]
	Threshold	90%	Almansouri et al. [46]
	Threshold	96.86%	Lopez et al. (2018)[59]
Machine Learning	CNN	65%	Cano et al. [67]
	KNN	Upto 95.35%	Hayawi & Waleed [66]
	Adaptive K-means	89.9%,	Molina-Cantero et al. [17]
	MLP SVM	80%,& 93%	Kabir et al. [49]
	Peak Detection	93.11% (Healthy), 85.14% (Patients)	Latifoglu et al.[16]
	SVM	89.1%	Masai et al [26]
	CART	>95%	Zaeni et al. [19]
	Real-time detection	87.67%	Lin et al. [53]
	Cuvic SVM	93.5%	Asanza et al.[13]
	Deep Learning	90.47%	Zou and Zhang [57]
	Inception	>96.4%	Hossieny et al. [58]
	SVM	90%	Martínez-Cerveró et al. [60]

vice for disabled patients. This device acquired EOG utilizing a custom-designed electronic module and processed the EOG in an Arduino Leonardo microprocessor board. This device utilized two adaptive thresholds for each channel. Four types of movement were detected based on the threshold. The average accuracy obtained was 90%.

Borkar et al. [22] used EOG to control a wheelchair. The wheelchair moved in the direction of eye movement such as left, right, up, and down. This work employed a thresholding algorithm.

Bastes et al. [65] developed a wearable single-channel EOG based HCI. EOG signals were conditioned by a hardware system and processed by software using a DFT-based algorithm. This design provided 90% accuracy.

Ryu et al. [24] used a new electrode positioning scheme to reduce the discomfort of users and removed baseline drift and noise with a differential EOG signal based on a fixation curve (DOSbFC). The proposed algorithm calculated the difference values of accumulated EOG signals between the initial eye movement and fixation time. The accuracies of the band pass filter and wavelet transform were 61% and 64% respectively. However, an average accuracy of 94% was found for eye movement detection.

Hou and Smitha [47] developed a low-cost wireless EOG based speller with dual channel EOG. A threshold algorithm was implemented on the Arduino to classify up to 10 different types of eye movements. The classified eye movement data were transmitted to a virtual keyboard. The proposed system showed accuracy of 89 % and a speed of 6.48 letters per minute.

Chowdhury et al. [21] proposed a threshold approach to control an wheelchair by directional eye movement information obtained from dual channel EOG signal. The classification stage incorporated threshold algorithm and was implemented in At-mega328 microcontroller. The data was acquired for different subjects. The accuracy of the proposed method was 96% during forward movement and 98% during stopping the wheelchair.

Prabha et al. [63] used horizontal EOG signal for movement of the hand for a paralyzed person. This signal was fed as an input to the microcontroller. A suitable program of conditional statements classified the movement. The output of the microcontroller was fed to the servomotor of the glove to control the hand.

Lopez et al. (2019) [64] utilized horizontal EOG for evaluating ataxic disorders. The developed system used conditional statements for classification of obtained data and showed 81.3% sensitivity, 85.7% specificity, and 83.3% accuracy.

Shivaprasad and Vishwanath [48] designed and implemented an EOG signal acquisition system. The new threshold algorithm developed in this work required much less user training than other classification algorithms. The developed HMI was able to generate control signals during various eye movements and blinks. which later were utilized for controlling the electric device model.

Savastaer and Tepe [23] designed and implemented a single-channel EOG amplifier circuit. Accuracies for for blink, up, and down are 91%, 94%, and 97% respectively using threshold.

Kishore Kumar and Narayanam [20] used an efficient Haar wavelet transform architecture for denoising the raw EOG signal The modified VLSI hardware architecture method detected the saccade and blink efficiently. Total on chip power consumption for all the stages was 225 mW. The number of used look up table and filp flops were 802 and 417 respectively.

Gundugonti and Narayanam (2021) [55] presented an architecture for saccade and blink detection. An efficient Haar discrete wavelet transform architecture using Radix-2r multiplier and 4:2 compressor was implemented. The Haar structure was synthesized in the Cadence RTL compiler. The proposed architecture had a delay of 7.09 ns and a power consumption of 2.71 mW.

Parra et al. [54] developed a portable EOG device. The signal acquisition, hardware, and software modules were integrated into a board prototype. The device was able to determine the direction of eye movements, such as up, down, left or right, and also blinks utilizing conditional statements. The efficiency of different

digital filter methods was verified and Coiflet5 for horizontal signals and coiflet4 for vertical signals stood out among all the methods.

Golparvar and Yapici [50] developed a graphene textile-based personal assistive device. Limitations of conventional wet electrodes were overcome in the device. The single-channel EOG data was processed using a microcontroller. Thresholds and other techniques were adopted for the classification of eye movements. Five different eye movements helped in tracking and operating remote objects. It was further utilized in a virtual keyboard and navigation of a robot. Typing speed accuracy up to 100% was achieved.

Anuradha et al. [56] presented a system for controlling electrical lights utilizing EOG signals. Conditional statements detected the blink using a microcontroller and are further used in controlling the lights. The overall accuracy of the system was 98%.

Daou et al. [43] presented a system to control the slide show using only eye movements. A particular movement in the eye allowed a change in the slide. Biosensors, electronic circuits as well as a microcontroller were deployed to recognize eye movement. A wireless signal was sent to the computer in order to move the presentation up or down. An overall accuracy of more than 90% was found in this work.

Li et al. (2022) [27] proposed a system named SmartLens to achieve eye activity sensing using zero-power contact lenses. A dedicated antenna was designed which fitted in a very small space and worked efficiently in more than 1 m distance. The accuracy of this work for detecting basic eye movement and blinking were at 89.63% and 82% respectively.

Abdel-Samei et al. [51] presented an EOG acquisition system based on Arduino microcontroller. A PCB based acquisition circuit was developed for dual channel EOG acquisition. Data was transferred from master to slave circuits with the NRF24L01 - 2.4G wireless transceiver module. The L298N driver circuit was mounted on a special robotic arm. This work used a threshold algorithm to detect

eye movements from EOG that were later used for robot control.

Almoansouri et al. [46] presented a magnetic eye tracker built by placing a composite magnet on the eyelid. The system detected down, up, left, or right using a threshold algorithm with 90% accuracy. Lopez et al. (2018) [59] developed a system to control a serious computer game using EOG signal. The designed system consisted of EOG acquisition circuit, digital processor, and game controller with eye movements. Fourteen volunteers tested the computer game. This system obtained around 96.86% accuracy using a threshold algorithm.

Cano et al. [67] presented an solution of SpinoCerebellar Ataxia type 2. The convolutional neural network of the design contained two convolutional layers (with ReLu nonlinearity and max-pooling) and two fully connected layers. All parts were integrated into an FPGA device. The achieved accuracy was 65%.

Hayawi and Waleed [66] implemented a driver assistance system utilizing the vertical acquisition method of EOG signals. An embedded system based on the ATmega2560 microcontroller on the Arduino was used to implement the EOG signal acquisition circuit. The system used K Nearest Neighbors classifier (KNN) and achieved maximum accuracy of 95.345% from 90% training and 10% testing.

Molina-Cantero et al. [17] used an acquisition circuit as in the single channel (vertical) method. A notch filter of 50 Hz was utilized to eliminate line interference. The adaptive K-means algorithm was used to recognize short or long blinks. The accuracy achieved for people without disabilities was 97.2% with double blinks, upto 76.6% for long blink and of 89.9% considering three classes.

Kabir et al. [49] extracted the EOG signal using the dual channel acquisition method and processed it for controlling cursor movement. Support Vector Machine (SVM) and Multilayer Perceptron (MLP) were used to classify different eye movements. The average accuracy of 93% was found across all directions.

Latifoglu et al. [16] designed an electronic circuit to acquire dual channel EOG and developed a system for diagnosing attention-deficit hyperactivity disorder (ADHD). An attention test with visual stimulus software was developed. The

stimulus images on the screen were monitored by eight patients with ADHD and eight healthy subjects during EOG recording. The accuracy for healthy individuals and patients was 93.11% and 85.14% respectively.

Masai et al. [26] used the eye-based interaction for facial expression recognition. They developed customized printed circuit boards (PCBs) for sensor units and microcomputer units. Three eye-based interactions were evaluated with the device. The average accuracy of detecting seven different eye gestures using SVM was 89.1%. The horizontal and vertical movements showed 58.8% and 82.4% accuracy respectively.

Zaeni et al. [19] used eye activity command to control the system in the patient room. A decision tree was designed to detect left gazes, right gazes, blinks, and double blinks. The decision tree model showed an accuracy of 99.9% and 98.87%, respectively in training and testing. By ignoring and obeying the no-action instruction, the model had an accuracy of 93.47% and 97.72%, respectively.

Lin et al. [53] developed a dual-channel data acquisition system using PCB. MSP430 F1611 was used as the main controller. The proposed algorithm detected different eye states and eye movements. The best subject performance achieved in this work was 96% and the average classification rate was 87.67%.

Asanza et al. [13] utilized dual channel EOG signals. They proposed SVM algorithm for six class classifications and achieved 93.5% accuracy. Then, a custom hardware architecture was developed for real-time implementation of the EOG classification model in al FPGA card.

Zou and Zhang [57] proposed a deep learning framework for automatic feature learning and classification. They also developed an edge computing platform on the smartphone to execute the deep learning algorithm and visualize the brain visual dynamics. They achieved a high eye-word recognition rate of up to 90.47%.

Hossieny et al. [58] detect six eye movements (up, down, right, left, double blinking, and center) from dual channel EOG. Three deep learning models: convolution neural network (CNN), visual geometry group (VGG), and inception had

been examined on filtered EOG signals. The inception model showed the best average accuracy of 96.4%.

Martínez-Cerveró et al. [60] used EOG for classifying four directions of eye movements. The system was based on open-source ecosystems, the Raspberry Pi single-board computer, the OpenBCI biosignal acquisition device, and an open-source Python library. They achieved a 90% accuracy using the SVM classifier.

2.7 Summary

The systematic review of the state-of-the-art verifies the use of EOG signals in multi-purpose applications. Most of these works are at the software level. Few works have been done at the hardware level based on EOG signal but they have some limitations in their studies as described in the literature review. There is a noticeable limitation in efficient FPGA implementations of machine learning based EOG signal classifications. Therefore, this thesis aims to develop this type of system for detecting blink and various eye movements.

Chapter 3: Software Backend

To design a digital system for processing EOG signals, first, a software backend is needed to be developed. This chapter discusses the algorithmic design of EOG signal processors for blink detection and eye movement classification. Section 3.1 describes the background of software designs of blink detection and eye movement classifications. Section 3.2 shows the brief methodology of this work. Section 3.3 briefly describes the used two datasets. Section 3.4, 3.5, 3.6, 3.7 represents the detailed description of the preprocessing, feature extraction, feature reduction, and classification stages of the software backend. respectively. Finally, Section 3.8 summarizes this chapter.

3.1 Background

Various medical conditions such as strokes, spinal cord injuries, amyotrophic lateral sclerosis (ALS), locked-in syndrome (LIS), etc. render patients paralyzed [17, 75]. Paralyzed people are unable to move the affected parts of the body either partly or entirely. They face difficulties in performing routine activities and communicating with the external world which impacts their quality of life [76]. Therefore, scientific researches are going on to ease the life of these partially or fully disabled people by creating an alternative form of communication.

Human-machine interfaces (HMIs) also known as human-computer interfaces (HCIs), can be helpful in this regard connecting the human body with the external environment [75]. Generally, HMIs utilize electro-physiological signals such as electroencephalogram (EEG), electromyogram (EMG), and electrooculogram (EOG) [77, 78]. Low power implemented HMIs integrated into portable applications can facilitate paralyzed people [79]. However, designing HMIs includes various algorithms in different signal processing stages resulting in complexity

for hardware realization. Thus, there are scopes for research in efficient hardware implementations of HMI.

Recently, EOG based HMI has emerged as a promising technology [9,80]. EOG has the information of eyes representing various eye movements. Eye movements can be considered an essential element used to express the desires, emotional states, and needs of people [81]. Therefore, translating EOG can greatly help people with major disabilities. The major advantages of EOG include non-invasive behavior, consistent signal pattern, and low cost [11,82].

EOG contains information of eye movements: blinks, saccades, and fixation. Blinking refers to an act of shutting and opening the eyes very quickly. Saccades are rapid movements of the eye that change the point of fixation. Fixation refers to the interval between two saccades. During fixation, the eyeball is fixed to the focus. The blinking information from EOG is utilized in many healthcare and technological applications. Some of them includes communication technologies [17], brain–computer interface (BCI) [83], fatigue detection [84], drowsiness detection [66], computer vision syndrome detection [85] etc.

On the other hand, in many applications of EEG signals, eyeblinks can contaminate the original information [86,87]. As the blinks are uncontrollable and involuntary activity, they can create EOG artifact. Accurate detection of blinks can be beneficial in denoising EEG signals in such cases. Therefore, designing an efficient blink detector is necessary.

Blinking and saccade information can be derived from EOG using various algorithms either using machine learning approaches or traditional approaches. Banerjee et al. [88] detected blinks utilizing RBF Kernel space vector machine (SVM) algorithm and achieved 95.33% accuracy. Ryu et al. [24] adopted a differential EOG signal based on a fixation curve (DOSbFC) to remove baseline drift and noise. They achieved 94.3% accuracy in detecting blinks, horizontal saccades, vertical saccades, and fixation. Molina-Cantero et al. [17] utilized adaptive K-means for classifying single blink, double blink, and long blink with 89.9%

accuracy. Gundugonti and Narayanam [55] detected blink using Haar discrete wavelet transform architecture using Radix-2r multiplier and 4:2 compressor to detect blink.

EOG signals can contain information on various eye movements along with blinks. This information can include up, down, right, left, and no movement. Multi-class classifications of eye movements are also important as they can be utilized in various HMI. In literature, a number of works classify EOG that include algorithms such as thresholding [89], support vector machine (SVM) [13, 79], k-nearest neighbors algorithm (KNN) [66], adaptive k-means [17], classification and regression tree (CART) [19], multilayer perceptron (MLP) [49,] convolution neural network (CNN) [67], deep learning neural network (DNN) [57], etc.

In this work, blinks and are detected using linear SVM binary classification. Then, six eye movements (up, down, normal, right, left, and blink) are detected using linear SVM multiclass classification.

3.2 Methodology

The goal of this thesis is to develop hardware-friendly algorithms to classify EOG signals and implement them in hardware. At first, the software simulation is needed to get insights into the algorithm. So, the systems have been designed in the software backend first. At first, the EOG data needs to be pre-processed as it is generally contaminated with high-frequency motion artifacts, power line interference, and baseline wander. The preprocessed data will be sent through the feature-extraction stage. The selected features after reduction will be used for classification. In the software design, various classifiers are checked to achieve better accuracy. As this thesis opts for hardware-software codesigning, it is needed to choose hardware-friendly features and classifiers i.e. the features and classifiers that will require a low number of hardware resources and will consume low power. Then, we can develop an efficient EOG Signal processor for FPGA implementation using the selected features in the classifier.

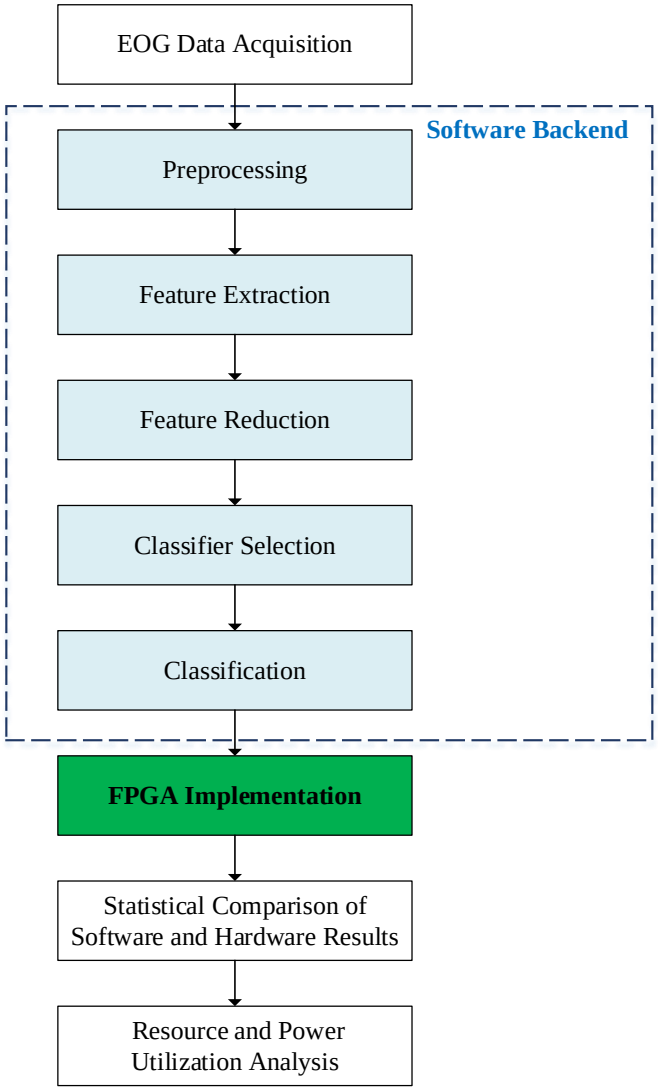


Fig. 3.1 Basic steps of designing FPGA implemented EOG processor

The basic steps of designing an FPGA implemented EOG processor using a machine learning approach are illustrated in Fig. 3.1. In this thesis, two systems are developed. The first system is designed for detecting blink that requires a binary classification of blinks and saccades. The second system detects six different eye movements: up, down, left, right, blink, and no movement (fixation). utilizing a multiclass classification of EOG Signals. For both designs, the software backend is developed first. This chapter discusses the software backend. The upcoming contents include the used datasets, the preprocessing stage, feature extraction, and reduction, and then the classification of the designed systems.

The complete software design for binary and multiclass classification is represented in a simplified block diagram of Fig. 3.2. Both designs include the basic stages of data acquisition, preprocessing, feature extraction, reduction, and classification.

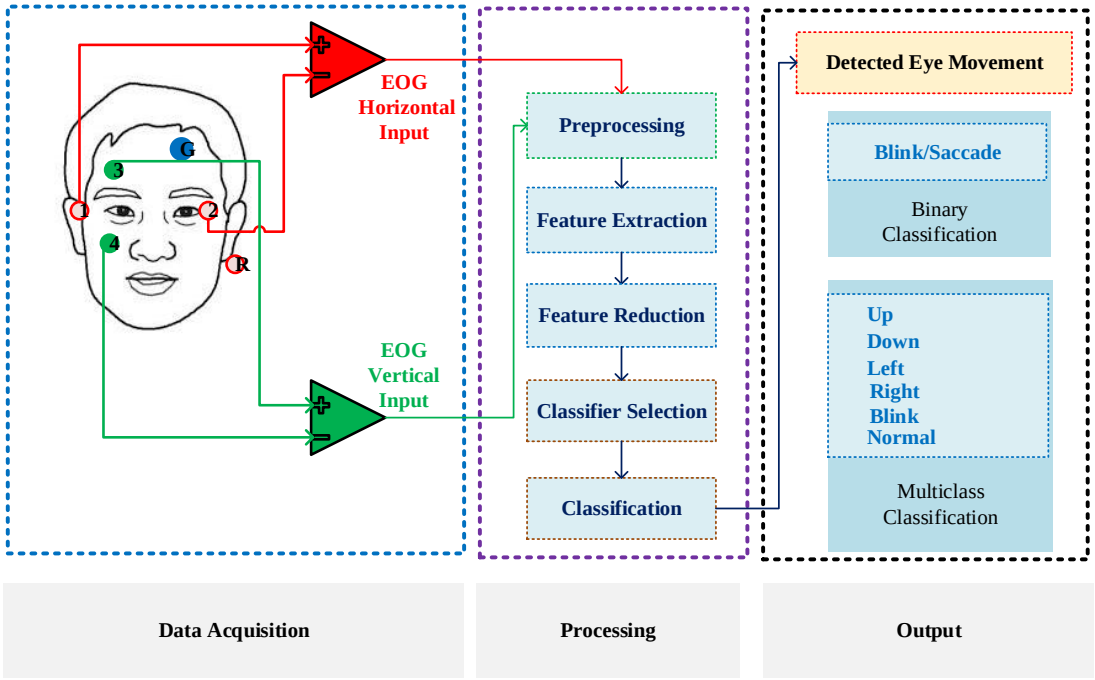


Fig. 3.2 Simplified block diagram of the complete system at the software level

3.3 Datasets

In this section, the two datasets used in the processor design are described. Dataset 1 is used in binary classification and dataset 2 is used in multiclass classification.

1. Dataset for Binary Classification

   In this work, the EOG signal from the eye movement EOG dataset is used [90]. It contains blink and saccade information on a total of six subjects. The EOG signals are recorded with a sampling frequency of 256 Hz. The EOG data consists of horizontal and vertical EOG signals. From this dataset, a total of 5400 epochs are generated for blink and saccades. These epochs are used for extraction of features which are later used in binary classification.

2. Dataset for Multiclass Classification

   The public dataset Electromyography (EMG) of the Extraocular Muscles (EOM) from IEEE Dataport [91] is used in this work. This EOG data consists of horizontal and vertical EOG signals. This dataset includes data from 10 subjects. All the subjects performed 10 pseudo-random repetitions of each of the following eye movements during the experiment: Up, Down, Right, Left, no movement (fixation in the center), and blinking. For each movement total of 100 epochs each of 2s is available. So, in total 600 epochs with labels are given for six eye movements.

3.4 Preprocessing

Preprocessing is the first stage of EOG processor design. It is necessary to prepare the data before sending it to the application stage as the raw data suffers from some unwanted noises. The noises are generally caused by three factors: the movement of other muscles near the eyeball, the electrical network operating at 50/60 Hz, and the continuous component of the signal.
The frequency range of EOG can be considered in the 0 to 30 Hz range or 0 to 40 Hz range. Therefore, it is desired to keep the frequency component of this range and eliminate other components. Therefore, filters are used for denoising the raw EOG signals from both datasets.

Here, the specifications of the filters are selected based on the recommendation of the dataset provider. However, in this work, it is always possible to reconfigure the specifications as necessary. Therefore, the filter specifications can be adjusted depending on the application.
In this work, for binary classification, the raw EOG data is obtained from dataset 1. The EOG signals of this dataset is preprocessed using two finite impulse response (FIR) filters: a high pass filter (HPF) with 0.03 Hz cutoff frequency, and a low pass filter (LPF) with 30 Hz cut-off frequency. The HPF is a constrained-

Table 3.1: Specifications of filters for Binary and Multiclass classification

	Specifications for Dataset 1		**Specifications for Dataset 2**	
Type of Filter	High-Pass FIR Constrained-least-squares	Low-Pass FIR Equiripple	High-Pass FIR Constrained-least-squares	Low-Pass FIR Equiripple
Sampling Frequency	256 Hz	256Hz	125 Hz	125Hz
Cutoff Frequency	0.03 Hz	-	0.5 Hz	-
Passband Ripple	0.02	-	0.02	-
Stopband Ripple	0.008	-	0.008	-
Passband Frequency	-	10 Hz	-	30 Hz
Stopband Frequency	-	30 Hz	-	40 Hz
Stopband Attenuation	-	60 dB	-	60 dB
Filter Order	26	25	24	24

least-square filter with an order of 26. Constrained-least-square filter are chosen as this type of filtering technique is feasible to filter out the baseline wander noise [92]. The LPF is an equiripple filter with an order of 25. The equiripple method is chosen as it meets the specifications without overperforming [93]. This method shows equal ripple in the pass band and stop band. Therefore, in the case of the lowpass filter, an equiripple filter is adopted.

The orders of the filters are chosen with minimum order to obtain the desired frequency response. Choosing a higher filter order number than the selected ones will require more resources and thus more power will be consumed. The high pass filter is capable of baseline drift mitigation [90]. The low pass filter denoised the raw signal to achieve the useful EOG component which lies below 30 Hz.

Table 3.1 summarizes the specifications of filters for binary classification and multiclass classification.

For dataset 2, the sampling frequency is 125 Hz. The filters are designed using

the same type of filters. The cut-off frequency is kept at 0.5 Hz for HPF. The pass-band and stopband frequencies are 30 Hz and 40 Hz respectively. In this case, the orders are found 24 to achieve the desired output in the preprocessing stage.
A pilot study was carried out to test the influence of the gender or age of the subject on the obtained EOG signal[94]. According to the experimental results of statistical analysis, the raw data did not show any significance in categorizing male-female or different age groups. Therefore, the filter properties can be kept the same for different age groups and for a wide range of age groups in the pre-processing stage.

3.5 Feature Extraction

The choice of features to extract from EOG signals depends on the specific research or application goals. Researchers and engineers often select or develop features that are most relevant to their particular use case. In general, the features extracted from EOG signals can be classified into three categories.

1. Time-domain features

   Time-domain features extracted from Electrooculography (EOG) signals are statistical and waveform-based characteristics of the signal that describe its behavior in the time dimension. These features can provide insights into eye movements, blinks, and other physiological phenomena. mean, variance, standard deviation, root mean square, skewness, kurtosis, etc. are some time-domain features that are used in combination with other domain-specific features and machine-learning techniques to analyze EOG signals for various applications.

2. Frequency-domain features

   Frequency-domain features are derived from the frequency components of a signal and are often used in signal processing and analysis to extract information about the underlying oscillatory patterns and periodicities. Fre-

quency domain analysis of EOG can reveal characteristics related to eye movements. Power Spectral Density (PSD), Spectral Entropy, Frequency Coherence, etc. are some common examples of frequency-domain features.

3. Time-frequency hybrid features

   Time-frequency hybrid features combine information from both the time domain and the frequency domain to capture the temporal variations in frequency content in the signals. These features are particularly useful when analyzing signals with non-stationary or time-varying characteristics. It can be useful for detecting dynamic eye movement patterns from EOG signals. Some common time-frequency hybrid features are short-Time Fourier Transform (STFT) features, Wavelet Transform features, Time-Frequency Bandwidth, etc.

The first objective of this thesis is to develop hardware-friendly algorithms for EOG processing. Therefore, the features considered are intended to be computationally simpler and less demanding to ensure lower hardware resource utilization and power consumption.

Among the three categories of features mentioned above, time-domain features present the most straightforward calculation option as they do not require heavy resource-demanding FFT, wavelet, or similar transformation techniques. In practice, time-domain features are extensively used in engineering and medical research, not only in the hardware domain but also in software counterparts, because their lower computational complexity leads to faster processing as well. Here, the preprocessed horizontal and vertical EOG data are utilized for selecting features. The preprocessed data of six subjects are segmented into small epochs. These epochs either carry saccade or blink movement. For feature selection, a number of statistical features have been checked. These features are:

- Mean: Mean is a statistical feature that refers to a measure of central tendency. It is often called the ”average” and is used to describe the typical or central value in a set of data points. The mean is calculated by adding up

all the values in a dataset and then dividing that sum by the number of data points. Mean is the average value of all the samples in a signal. The mean of a vector **x** containing N scalar observations, can be found using Equation (3.1)

$$\bar{x} = \frac{1}{N} \sum_{i=1}^{N} \mathbf{x_i} \tag{3.1}$$

- Mean Absolute Deviation: The Mean Absolute Deviation (MAD) provides a measure of the average distance between data points of a vector and the mean. It is a useful statistic to understand how spread out the data is. The Mean Absolute Deviation of a vector **x** containing N scalar observations, can be found using Equation (3.2)

$$x_{MAD} = \frac{1}{N} \sum_{i=1}^{N} |x_i - \bar{x}| \tag{3.2}$$

- Root Mean Square: Root Mean Square (RMS) is a statistical measure used to find the average value of a set of values. It is often used in the context of signal processing, statistics, and mathematics. It is particularly useful for calculating the root average of a set of values, especially when dealing with varying magnitudes. The root-mean-square level of a vector **x** containing N scalar observations, can be found using Equation (3.3).

$$x_{RMS} = \sqrt{\frac{1}{N} \sum_{i=1}^{N} |\mathbf{x_i}|^2} \tag{3.3}$$

- Standard Deviation: Standard Deviation is a statistical measure of the amount of variation or dispersion in a set of values. It quantifies how spread out or how much the values in a data set differ from the mean (average) of that data set. It informs how much individual data points deviate from the mean. For a random variable vector **x** containing N scalar observations, the

standard deviation is defined as Equation (3.4).

$$\sigma = \sqrt{\frac{1}{N-1}\sum_{i=1}^{N}|\mathbf{x_i} - \bar{x}|^2} \tag{3.4}$$

where $\bar{x}$ is the mean of **x** as given in Equation (3.1).

- Variance: Variance refers to the measure of the spread between samples in a dataset. The variance provides insights into the dispersion of the data points around the mean. A higher variance indicates that the data points are more spread out from the mean, while a lower variance indicates that the data points are closer to the mean. Variance is always a non-negative value. For a random variable vector **x** containing N scalar observations, the variance is defined as Equation (3.5).

$$variance, \sigma^2 = \frac{1}{N-1}\sum_{i=1}^{N}|\mathbf{x_i} - \bar{x}|^2 \tag{3.5}$$

where $\bar{x}$ is the mean of **x** as given in Equation (3.1).

- Skewness: Skewness is a measure of the asymmetry of the data around the sample mean. If skewness is negative, the data are spread out more to the left of the mean than to the right. If skewness is positive, the data are spread out more to the right. The skewness of the normal distribution (or any perfectly symmetric distribution) is zero. For a random variable vector **x** containing N scalar observations, the skewness is defined as Equation (3.6). It is expressed by:

$$Skewness = \frac{1}{(N-1) * \sigma^3}\sum_{i=1}^{N}(x_i - \bar{x})^3 \tag{3.6}$$

where, $\bar{x}$ is the mean of **x** as given in Equation (3.1) and σ represents standard deviation as given in Equation (3.4).

- Kurtosis: Kurtosis is a measure of how much of a variable distribution can

be found in the tails. It can determine how outlier-prone a distribution is. It can be defined as Equation (3.7).

$$Kurtosis = \frac{1}{(N-1) * \sigma^4} \sum_{i=1}^{N} (x_i - \bar{x})^4 \tag{3.7}$$

where, $\bar{x}$ is the mean of **x** as given in Equation (3.1) and σ represents standard deviation as given in Equation (3.4).

3.6 Feature Reduction

After calculating these features for both horizontal and vertical EOG signals, the number of features is reduced using the Maximum Relevance Minimum Redundancy (MRMR) algorithm [95,96]. This algorithm is very popular for classification problems. It tends to find an optimal set of mutually and maximally dissimilar features that can represent the response variable effectively [97]. Here, the

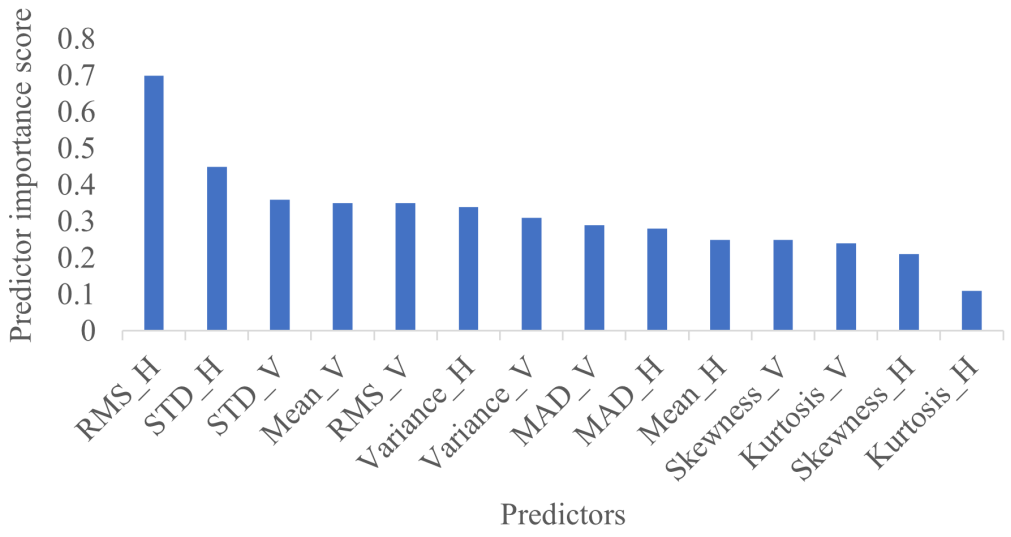


Fig. 3.3 Predictor importance score for features in binary classification

redundancy of a feature set is minimized and the relevance of a feature set to the response variable is maximized. The redundancy can be calculated using mutual information of features. The relevance can be assessed by the mutual information of a feature and the response. A detailed description of this algorithm is attached

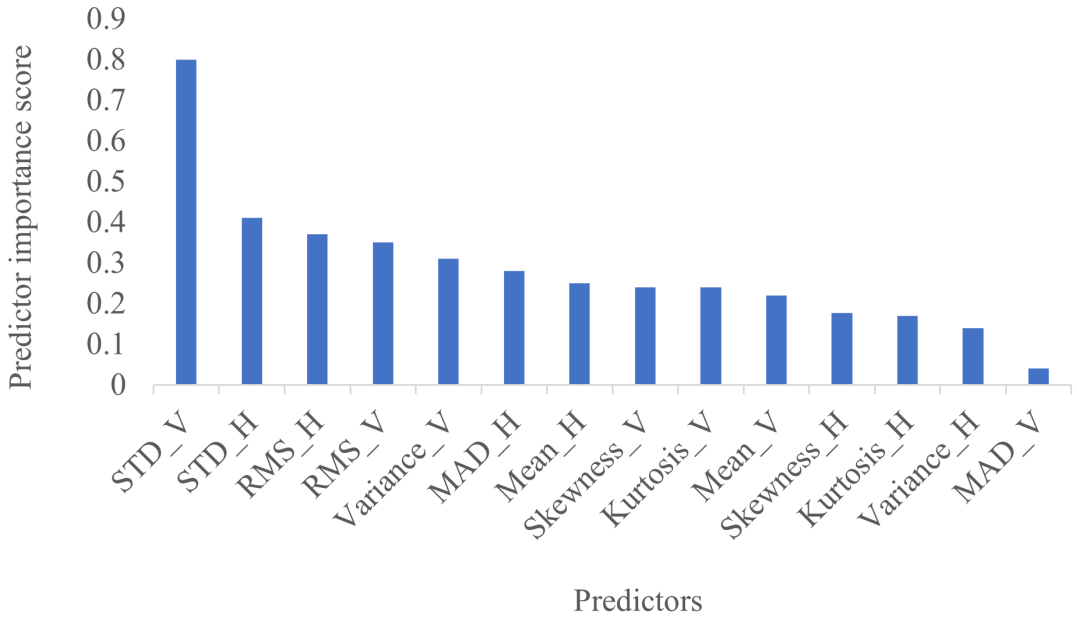


Fig. 3.4 Predictor importance score for features in multiclass classification

in Appendix B. The algorithm provides predictor ranks based on the predictor importance score. Fig. 3.3 and Fig. 3.4 show the predictor importance scores for features from dataset 1 and 2 respectively. As the binary and multiclass classification utilizes dual channel data, the chosen features are root mean square (RMS) and standard deviation (STD) for both channels considering the predictor importance score. RMS and STD are statistical measures that provide information about the dispersion or variability of data. In the case of Electrooculogram signals, the variability of the signals may contain valuable information that is relevant to the target eye movement. Additionally, RMS and STD are able to smooth out some of the noise and focus on the underlying patterns. These can be the possible reasons for yielding greater score than other features. These features are further utilized for classification.

3.7 Classification

A classifier in the machine learning approach refers to a type of algorithm or model that is trained to make predictions or decisions based on input data. Classifiers are a fundamental component of supervised learning. Supervised learning

Table 3.2: Software accuracies for different classifiers.

Classification	Algorithm	Accuracy
Binary	Tree	98%
	SVM	97.55%
	KNN	95%
Multiclass	Tree	88%
	SVM	97.92%
	KNN	90.20%

algorithms learns from labeled training data and is then able to classify new, unseen data points into predefined classes. Some common types of classifiers used in machine learning are: Decision trees, naive Bayes classifiers, k-nearest neighbors (k-NN), support vector machines (SVM), artificial neural networks (ANN), etc. are some commonly used machine learning algorithms. The decision tree algorithm uses a tree-like model that recursively splits the data into subsets based on features until a decision is reached. The naive bayes classifiers use a probabilistic classification algorithm that is based on Bayes' theorem with an assumption of independence among the features. k-NN is a simple machine learning algorithm that memorizes the training dataset. Then K-NN makes predictions for new data points by calculating the distance between this point and all the data points in the training dataset and selecting the k data points (neighbors) with the smallest distances to the new data point. ANNs are a class of machine learning models imitating function of biological neural networks, such as the human brain. ANNs consist of interconnected artificial neurons divided into input layers, hidden layers, and output layer. SVM algorithm finds the hyperplane that best separates different classes of data considering the maximum margin between them.
In this study, the aim is to design EOG processor with hardware-friendly algorithms. At first, tree, SVM, and KNN classifiers are checked at the software level using the extracted features. The accuracy of different classifiers at the software level is listed in Table 3.2.

At the software level, the decision tree shows maximum accuracy for binary classification. The second-best accuracy is achieved using linear SVM.

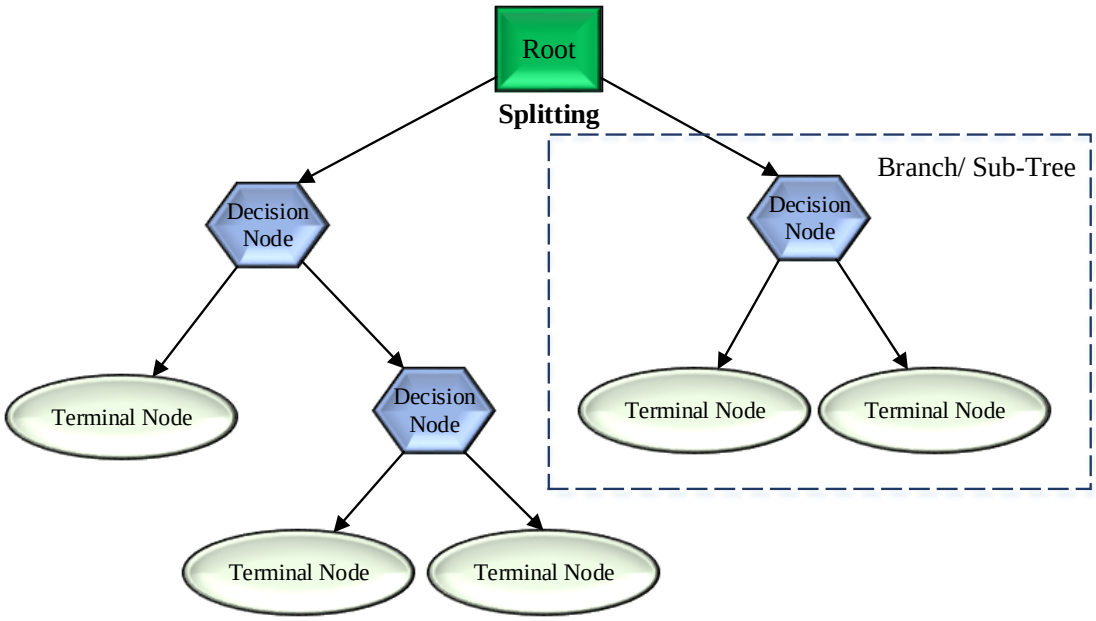


Fig. 3.5 Tree classifier

However, the tree classifier takes decisions by splitting the root node into branches, a number of checks, and then terminating as shown in Fig. 3.5. Tree classifiers with deep or highly branching structures may require high precision for accurate calculations. Software implementations can use arbitrary precision arithmetic if needed, which can lead to higher accuracy. FPGAs have limited resources in terms of logic elements, memory, and processing units. If the tree classifier is too large or complex to fit within the available resources, compromises may need to be made in the FPGA implementation, potentially leading to lower accuracy.

Therefore, linear SVM has been chosen for its efficient behavior by providing the desired accuracy that outperforms other known classifiers [98]. FPGAs can perform parallel dot product calculations, which are at the core of SVM computations. This parallelism can significantly accelerate SVM training and inference processes.

For multiclass classification SVM showed better accuracy than others. Therefore, it is chosen for implementation of multiclass classifier.

The binary classification and multiclass classification approaches of this study are described below.

3.7.1 Binary Classification

Binary classification is a basic task in machine learning and statistical modeling. The aim of binary classification is to categorize data points into one of two possible classes. In binary classification, each data point is assigned to one of two exclusive groups based on certain features. The decision boundary is a mathematical or algorithmic construct that separates the two classes in the feature space.

In this work, as a classification model SVM is chosen that provides a hyperplane

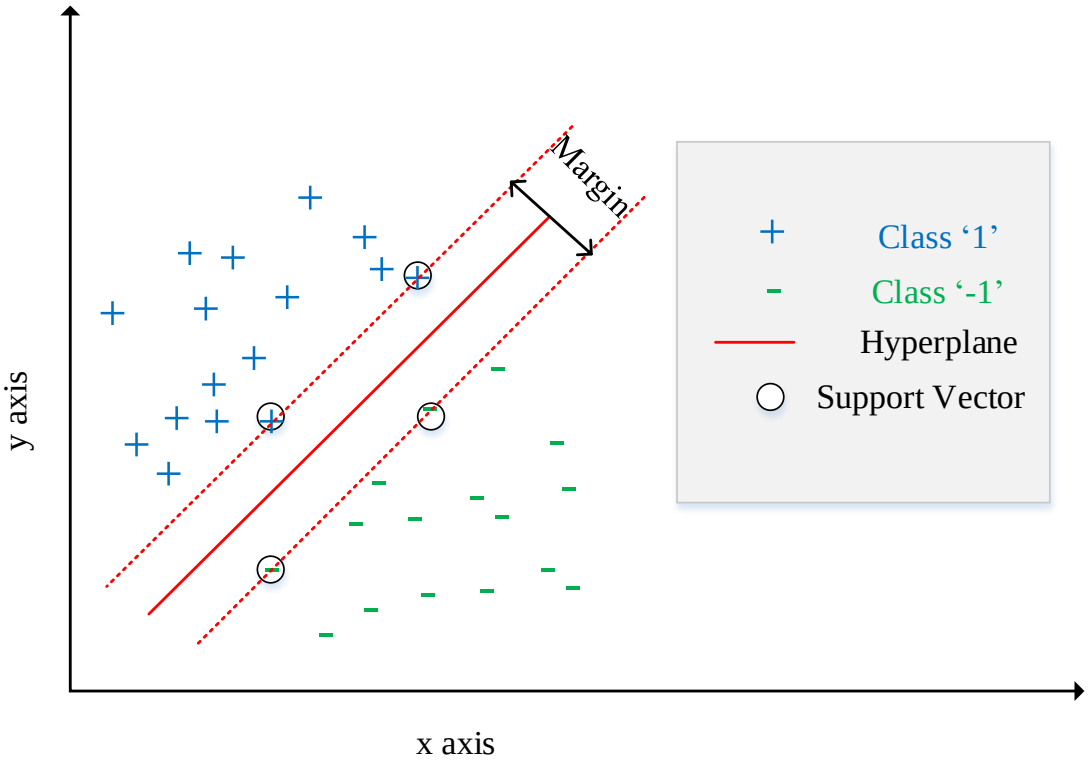


Fig. 3.6 Boundary between two classes defined by a hyperplane in SVM

to categorize the given data into two classes. SVM is one of the most effective machine learning algorithms, mostly used for pattern identification. SVM can be used for data that have an unknown distribution. The SVM model aims to maximize the margin between classes and at the same time, it minimizes classification errors. This margin-based approach often results in models that are less prone to overfitting, leading to better generalization of unseen data. SVMs can deal with both linearly separable and non-linearly separable data through the use of vari-

ous kernel functions. Kernel function is the mathematical function used for the transformation. Commonly used kernels include linear, polynomial, radial basis function (RBF), and sigmoid kernels.

In this work, the linear kernel is chosen. The selection is guided by the underlying data distribution and the results of model evaluation and validation. Fig. 3.6 shows that a hyperplane boundary defined by linear SVM categorizes the classes. The support vectors represent the data points that are closest to the separating hyperplane i.e. the points are on the boundary. The Fig. 3.6 illustrates these definitions, with + indicating data points of class 1, and – indicating data points of class –1.

The SVM classifier takes the features from the feature extraction stages as input and provides the class label as output using the equation. The labeling for blink is given as +1, and for saccade is -1. Theoretically, The SVM binary classification algorithm uses the scoring function given in Equation (3.8).

$$f(x) = x'\beta + b \tag{3.8}$$

where: x is an observation. The vector β contains the coefficients that define an orthogonal vector to the hyperplane, i.e. the weight values of the features and b is the bias term. The classifier output detects the eye movement either as +1 (blink) or -1 (saccade). The weight and bias values are given in Appendix C.

3.7.2 Multiclass Classification

SVM method can be used for multiclass classification. Theoretically, the SVM is a binary classification algorithm. The multi-class classification is based on multi-binary SVMs. One-vs-one and one-vs-all approaches can be adopted to realize multiclass SVM classification [98].

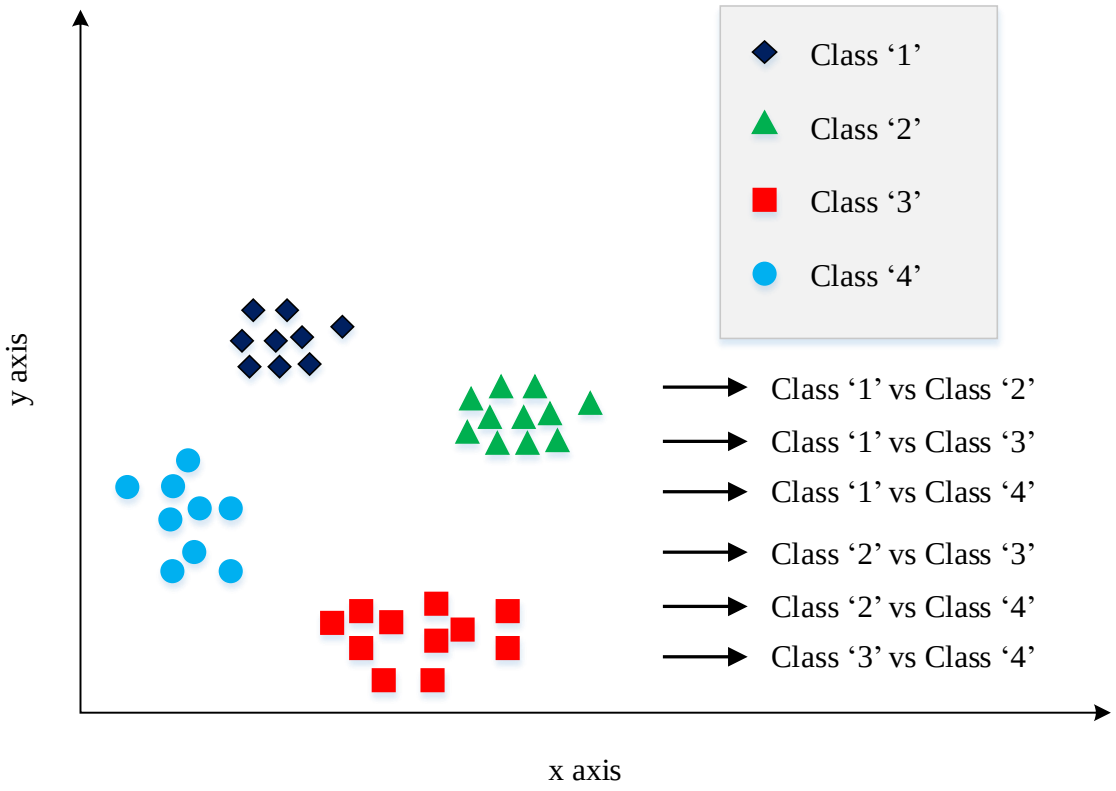


Fig. 3.7 One-vs-One approach in multiclass SVM

One-vs-One approach

The one-vs-one approach divides the multiclass classification problem into several binary classification problems. A binary classifier is trained for each pair of classes in the multi-class classification problem. If there are N classes, this results in N(N-1)/2 binary classifiers.

As shown in Fig. 3.7, for multiclass classification with one-vs-one approach, for each pair of classes, a binary classifier is designed. When making a prediction for an unseen input, each binary classifier votes for one of the two classes in the pair. The class that receives the most votes across all classifiers is then predicted as the final output. The drawback of this approach is that it can become computationally expensive as the number of classes increases.

One-vs-All approach

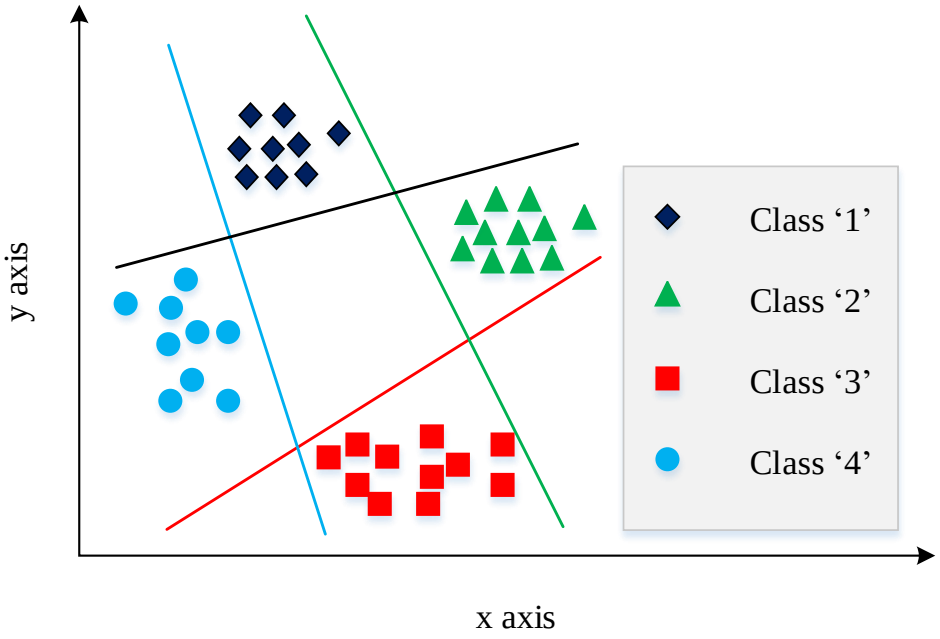


Fig. 3.8 One-vs-All approach in multiclass SVM

In the one-vs-all technique, a separate binary classifier is trained for each class in the multi-class classification problem. If there are N classes, this results in N binary classifiers. When making a prediction for an unseen input, each binary classifier determines whether the input belongs to its assigned class or not (i.e., it's a one-class vs. all others classification). The classifier with the highest probability is chosen as the predicted class. A hyperplane is required in the one-vs-all in order to simultaneously divide all classes from one another. This indicates that all points are considered, and they are split into two groups: a group for class points and a group for all other points as shown in Fig. 3.8.

The selection choice between one-vs-one and one-vs-all depends on the specific problem, the characteristics of the classifiers being used, and computational considerations. The one-vs-all approach trains less number of classifiers than the one-to-one approach. Hence, the computational time will be faster as well as less number of resources and power will be utilized for the one-vs-one approach. The

one-vs-all is more commonly used due to its simplicity and efficiency in practice, especially for problems with a large number of classes. Therefore, in this work one-vs-all approach is adopted to minimize the number of binary classifiers to optimize the hardware design.

The SVM classifier takes the features as input and provides the class label as output using the equation. Here, 80 percent data is used for training and 20 percent data is used for testing the SVM classifier. All parameters of the SVM models for binary classification and multiclass classification are given in Appendix C.

3.8 Summary

In this chapter software backend designs for binary and multiclass classification of EOG signals are explained step by step. These designs will be implemented in hardware in the upcoming chapter.

Chapter 4: Hardware Frontend

The software simulation of the Chapter 3 is needed to be translated in hardware for the digital implementation. This chapter describes the hardware frontend designs of each step for developing EOG processors. Section 4.1 contains a brief description of the background of EOG hardware implementations. As EOG is a dual-channel signal, it is important to get insights on the processing approaches of multichannel data. Section 4.2 describes the processing approaches in hardware. Section 4.3 discusses the methodology and design steps of the hardware frontend. Finally, Section 4.4 provides the summary of this chapter.

4.1 Background

Digital design can be defined as the process of designing electronic circuits, systems, or devices that have specific purposes to address needs in the field of concern. For digital desigining, hardware-software codesign play a vital role in verifying the performance. The codesign is an approach to design complex systems that integrates both hardware and software components from the outset to achieve optimal system performance, functionality, and efficiency. This approach recognizes that some tasks are better suited for hardware acceleration, while others are best implemented in software, and seeks to find the right balance between the two.

A digital blink detector can be considered as an EOG based point-of-care systems as it can be utilized in the diagnosis of diseases by monitoring the blink rate. These designs provide cost-effectiveness, quick monitoring, remote healthcare facilities, etc. [99]. Digital blink detectors can detect blinks in real time. These detected blinks can also be utilized in various applications in addition to disease detection. The applications may include drowsiness monitoring of drivers which

can save them from major road accidents, and fatigue detection in smart office workstations.

EOG-based digital systems can be designed using multiclass eye movements also. Software-based improvement is going on to classify eye movements from EOG over the past decade [14]. Hardware-based works of EOG are being given focus now. EOG can be implemented in non-reconfigurable hardware using PCB, micro-controllers, Arduino [51, 100], and also in re-configurable structures like Field Programmable Gate Array (FPGA) [11, 67]. FPGAs are integrated circuit (IC) that can be reconfigured for any assigned task. Therefore, they can be the proper solution for pragmatic embedded system design utilizing hardware resources effectively with low power consumption [101,102].

A popular approach to digital design is the application specific integrated circuit (ASIC). It is also known as an application specific processor or application specific integrated processor. ASIC refers to an integrated chip designed for a particular application [103]. These designs are seen in many advanced technologies and electronic devices. Application specific processors can be designed using field programmable gate arrays (FPGA). FPGA has advantages such as reconfigurable design capability, low latency, and low power [30,104]. FPGA allows custom-made circuit designing scheme. It is possible to speed up data processing using parallel architecture and minimize resource utilization using serial architecture. ASIC design in FPGA fixes the functionality and reduces the number of components used. Therefore, these compact design provides the benefits of low cost, high performance, and power efficiency.

ZedBoard is a low-cost development board manufactured by Digilent. This board employs Xilinx Artix-7 FPGAs coupled with a dual-core ARM Cortex-A9 processor [30]. The ZedBoard has a broad range of applications, such as digital signal processing (DSP), image processing, industrial automation, etc. This FPGA system-on-a-chip (SoC) based board enables the designers to accelerate the custom DSP algorithm, as it is possible to program Zedboard whenever necessary

[31]. In this thesis, Zedboard is used for implementing the EOG processor of the blink detection system. The second design of the multiclass eye movement classifier uses Zynq UltraScale+ as this design needs more resources than the binary classifier. ZedBoard and Zyng UltraScale+ are used as the processing unit for hardware implementation. The programming is done using System Generator, a design tool for the implementation of DSP algorithms in Xilinx devices.

4.2 Processing Approaches

In this work, two-channel EOG signals are used for the analysis. Theses two channel provides EOG horizontal signal and EOG vertical signal. The hardware frontend can be designed using two different approaches for multichannel signals. They are: serial processing, and parallel processing. A brief description of the approaches along with their advantages and disadvantages is given below.

1. Serial processing

   In serial processing, each EOG channel is processed one after the other, and the analysis for one channel is completed before moving on to the next. This approach is sequential and may be appropriate when the channels are largely independent of each other or when the computational resources are limited. The main two advantages of the serial processing approach include simplicity and interpretability. It is considered simple as it is straightforward to implement, especially for simple analyses. Each channel can be easily interpreted independently. However, serial processing is inherently slower because tasks are executed one after the other. Therefore, serial processing needs longer processing times for computationally intensive tasks. As a result, it often requires devices to remain active for longer periods making the energy consumption high. In addition, if one task encounters an error or fails, it can disrupt the entire process, potentially causing a system failure.

2. Parallel processing

   In parallel processing, all EOG channels are processed simultaneously or in parallel. This approach leverages the inter-channel relationships and can be more computationally efficient for tasks that require a joint analysis of all channels. For computationally intensive tasks, parallel processing can be more efficient, especially on multi-core or distributed computing platforms. However, implementing parallel processing with a large number of processing elements may not be feasible as FPGAs have limited hardware resources. In addition, high-performance FPGAs capable of parallel processing can be expensive, especially for large-scale projects that require multiple FPGAs.

The choice between serial and parallel processing depends on the specific research goals, computational resources, and the nature of the EOG data. Some tasks may benefit from a combination of both approaches, where certain preprocessing or feature extraction steps are performed in parallel, while others are done serially. The decision should be guided by the problem's complexity and the need for inter-channel information integration.

4.3 Methodology

Hardware-based designs require optimization for feasibility and low-cost implementation. Therefore, the system needs to be designed using a mathematically less complex software backend. The mathematical validation and primary simulation of this work are designed using MATLAB. The preprocessing stage uses digital filters with a minimum order to obtain the desired signal quality [11]. The statistical features are chosen based on correlation. The support vector machine (SVM) classification scheme is feasible for this work as it uses fewer resources than other classifiers. Then, the system is designed using the Xilinx system generator. The hardware design of the whole system consists of three main subsys-

tems: preprocessing, feature extraction, and classification.

The reconfigurable system is designed with a combination of serial-parallel processing for hardware optimization. At first, the horizontal and vertical EOG signals are taken as parallel input. The horizontal EOG is pre-processed, and then the vertical data is pre-processed serially. Then, both signals are normalized in parallel to speed up the whole operation. The preprocessed horizontal and vertical EOG signal features are extracted serially using one unit. A fast counter is used to minimize the operation time for serial processing.

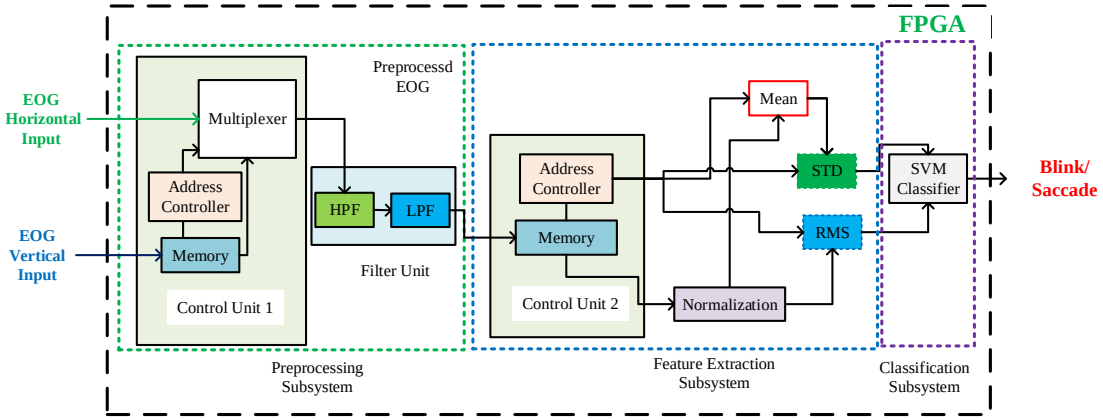


Fig. 4.1 Block diagram of the FPGA implemented system for Binary classification

The EOG processor for binary classification design is realized in hardware using ZedBoard. It is a low-cost development board that uses Xilinx Artix-7 FPGAs [30]. The software co-simulation is performed using Xilinx System Generator(XSG) in MATLAB Simulink Platform. The block diagram of the FPGA-implemented system binary classification system is depicted in Fig. 4.1. It takes horizontal EOG signal and vertical EOG signal as input and provides blink/saccade information after processing.

The complete hardware design of the EOG processor for multiclass classification is realized in hardware using Zynq UtraScale+. The FPGA implemented system is presented in a simplified block diagram in Fig 4.2. It also takes two-channel EOG signals as input and identifies one of the six eye movements.

The FPGA-implemented systems for EOG classification contain three subsystems.

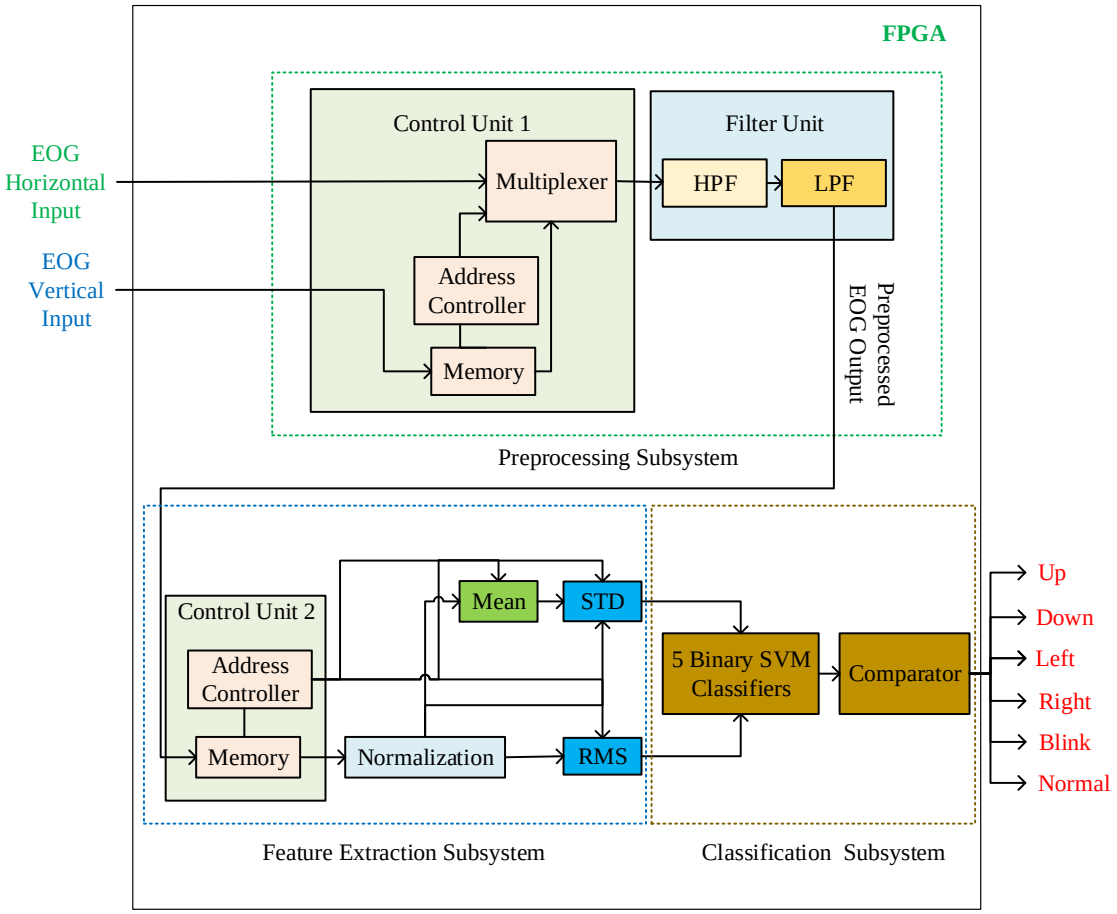


Fig. 4.2 Block diagram of the FPGA implemented system for Multiclass classification

- Preprocessing Subsystem
- Feature Extraction Subsystem
- Classification Subsystem

The main difference between the two designs is in the classification subsystem. The binary classifier needs only SVM classifier, whereas the multiclass classifier needs five SVM classifiers and one comparating logic.

FPGA designs can be done using both serial processing (pipelining quality) and parallel processing (parallelism quality). The designs of this thesis utilize a hybrid of pipelining and parallelism to achieve optimal performance [105]. The selection of design approaches for the above-mentioned subsystems is summarized in Table 4.1.

Table 4.1: Selection of processing approach for different stages

	Serial Processing	Parallel Processing	Reason	Frequency of Binary Classification	Frequency of Multiclass Classification
Data Acquisition		✓	Multichannel data acquisition at the same time	256 Hz	125Hz
Preprocessing Subsystem	✓		Resource Minimization	*256 Hz, **2.56 MHz	*125 Hz, **1.25 MHz
Feature Extraction Subsystem	✓		Resource Minimization	2.56 MHz	1.25 MHz
Classification Subsystem		✓	Features are provided in the classifier at the same time	2.56 MHz	1.25 MHz

*Horizontal EOG Signal, **Vertical EOG Signal

4.3.1 Preprocessing Subsystem

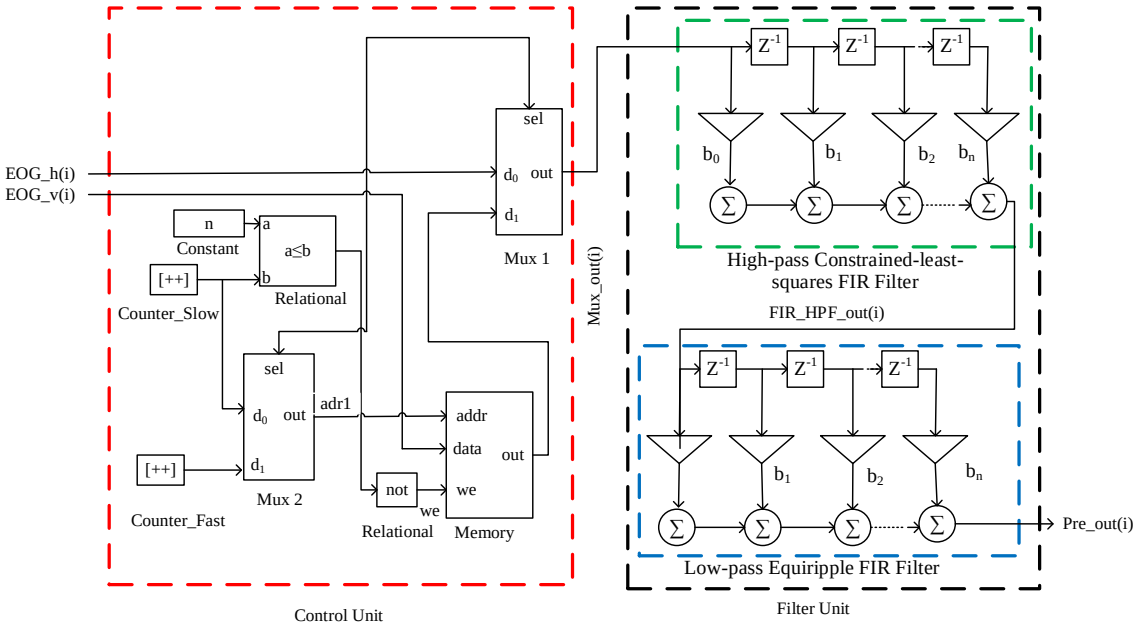


Fig. 4.3 Block diagram of the preprocessing subsystem

Fig. 4.3 depicts the block diagram of the preprocessing subsystem. It consists of a control unit (red) and a filter unit (black). The control unit takes horizontal data EOG_h(i) and vertical data EOG_v(i) as input and passes sequentially to the filter unit using a multiplexer, Mux 1. The output of the control unit Mux_out(i) is given as input for the filter unit. The control unit block has two up counters: Counter_Slow and Counter_Fast. These counters work at 256 Hz and 2.56 MHz respectively. The random-access memory (RAM) block stores the vertical data while horizontal data is preprocessed in the filter unit. The vertical data stored in the RAM is passed sequentially. Multiplexer 2 generates addresses for the memory block, RAM. The filter unit contains two filters designed using Matlab FDATool. The first filter is a high pass FIR constrained-least-squares filter with a 0.03 Hz cutoff frequency. The second filter is a low pass FIR equiripple filter with a 30 Hz cut-off frequency. The order of the filters is set as 26 and 25 respectively as mentioned in the Section 3.4. For processing the data for multiclass classification, the counters work at 125 Hz and 1.25 MHz respectively. In this case, the filter unit consists of a high pass FIR constrained-least-squares filter with a 0.5 Hz cutoff

frequency and low pass FIR equiripple filter with a 40 Hz cut-off frequency. The order of the filters is set as 24 for both filters as mentioned in the Section 3.4. The preprocessing subsystem provides Pre_out(i) as output.

4.3.2 Feature Extraction Subsystem

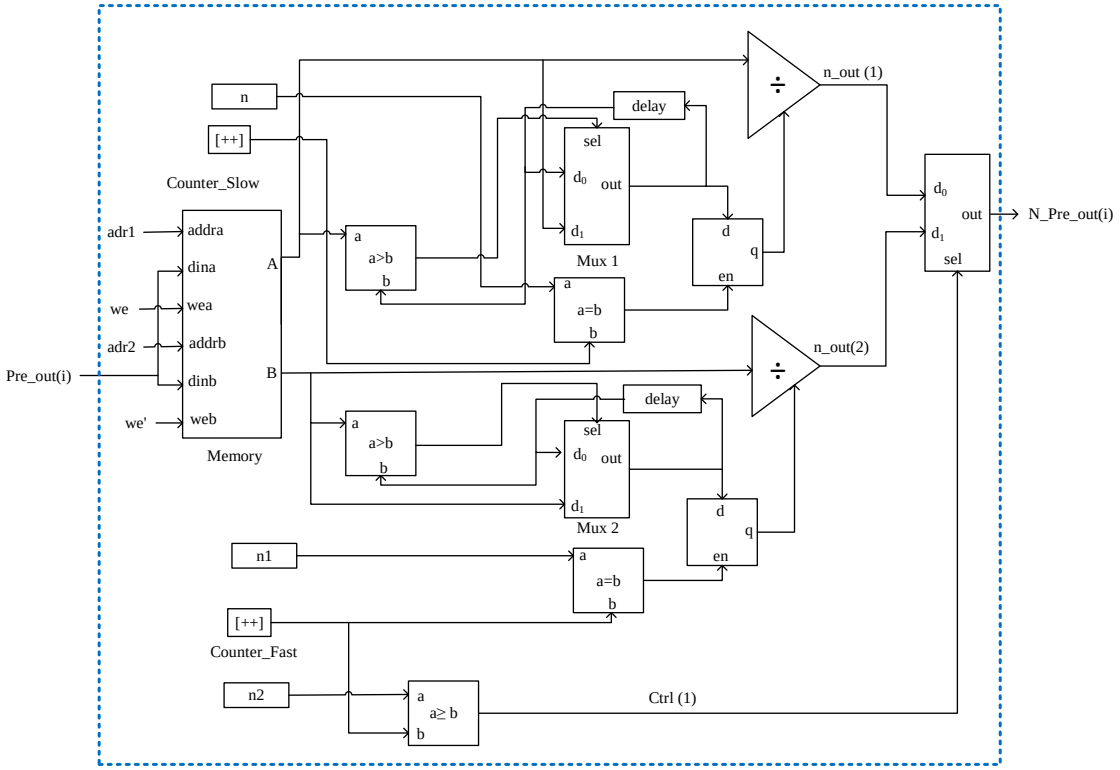


Fig. 4.4 Normalization of the preprocessed EOG signals

The Pre_out(i) signal from the preprocessing subsystem is normalized before sending it to the feature extraction stage. The normalization process is done as shown in Fig.4.4. The normalization process is designed using the parallel technique to speed up the operation. It takes Pre_out(i) of the preprocessing subsystem as input. This signal contains preprocessed horizontal and vertical EOG signals serially. So, generating addresses based on their position the data are stored in the dual-port RAM. In this case, control Unit 2 of Fig. 4.1 creates the address for the memory block using counters. Constants n, n1, and n2 represent the number of observations. These values are compared with the counter value at a given instant to create control signals that further enable registers as per the requirement

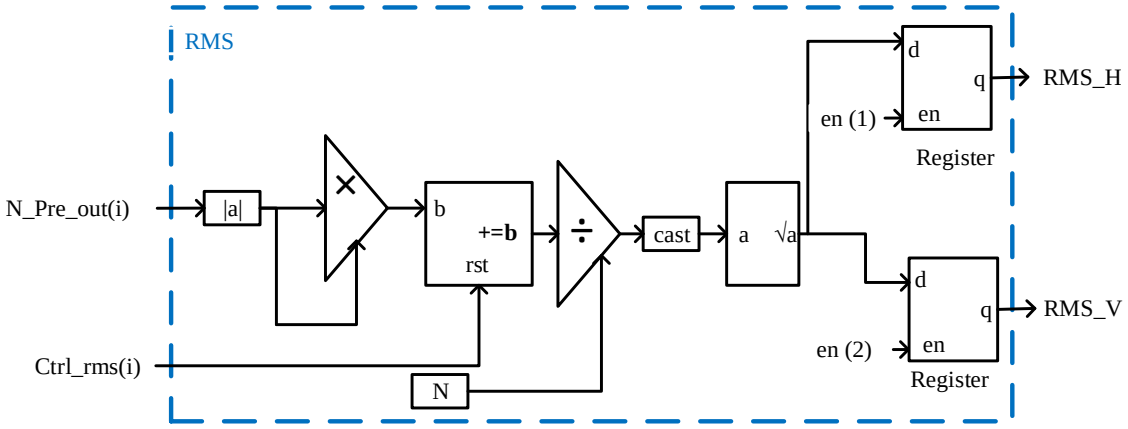


Fig. 4.5 Block diagram of the RMS calculator in feature extraction subsystem

and select the type of signal, either horizontal (d_o) or vertical (d_1) to be passed. This normalization block compares the value of the input signal at any instant with the value of its previous instant using delay and comparator blocks. If the new observation has a higher value than the previous observation it is passed and stored in the register otherwise the previous observation is unaltered in the register. So, after the given time the maximum value of the preprocessed EOG_h and EOG_v are found. Then the original preprocessed data stored in the memory block is divided by these maximum values returning parallel normalized EOG signals (n_out(1), and n_out(2)). These signals are later made sequential using a multiplexer resulting in the normalized preprocessed EOG signal, N_Pre_out(i). Then, two features: root mean square (RMS) and standard deviation (STD) are extracted.

Fig. 4.5 demonstrates the internal formation of the RMS calculator. The RMS features can be implemented using Equation (4.1).

$$RMS = \sqrt{\frac{1}{N}\sum_{i=1}^{N} |(N\_Pre\_out(i)|^2} \tag{4.1}$$

Here, N_Pre_out(i) represents a normalized preprocessed EOG epoch. N is the number of observations in Pre_out(i). In the RMS calculator block, the prepro-

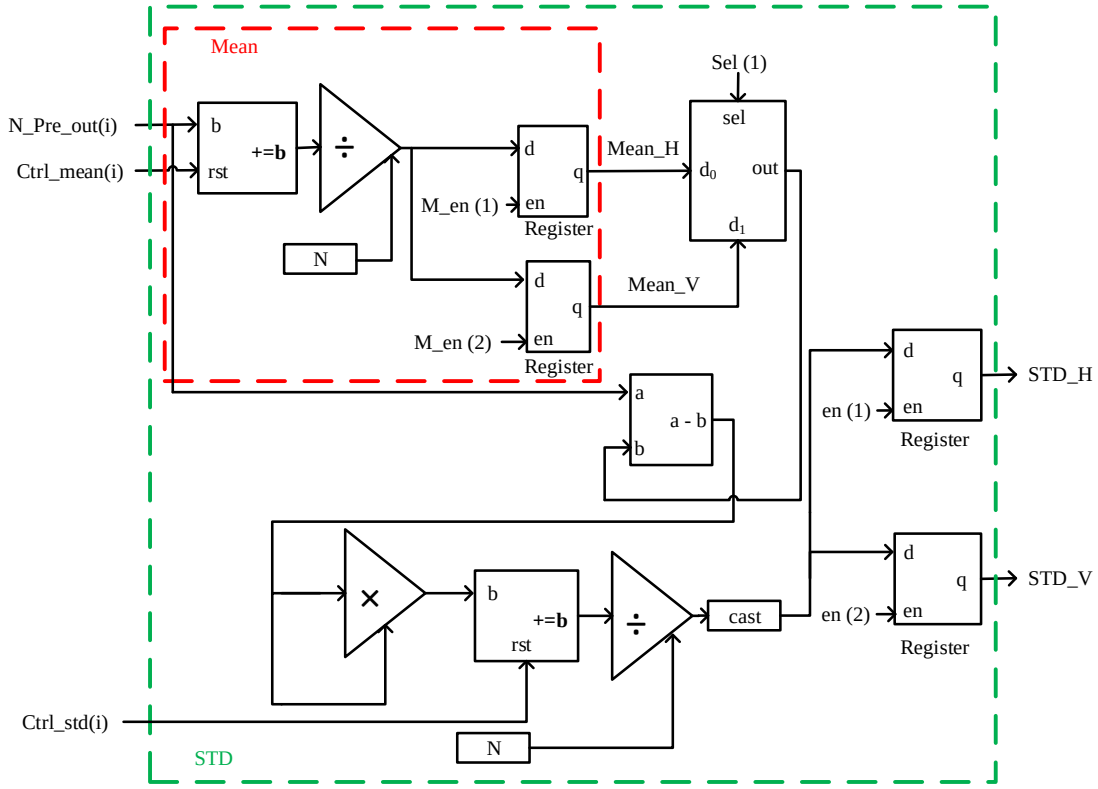


Fig. 4.6 Block diagram of the STD calculator in feature extraction subsystem

cessed EOG epoch, Pre_out(i) is squared. Then, the average of the squared term is calculated consecutively using a multiplier, an accumulator, and a divisor circuit. The RMS is obtained by the square root of this average squared term. The RMS_H and RMS_V are calculated in a serial manner and stored in the register. The control signal Ctrl_rms(i) helps in maintaining coherence in the process.

Fig. 4.6 illustrates the internal formation of the STD calculator. The STD features of all data are extracted using Equation (4.2).

$$STD = \sqrt{\frac{1}{N-1}\sum_{i=1}^{N}|N\_Pre\_out(i) - \mu)|^2} \tag{4.2}$$

Here, μ represents the mean. For the hardware implementation, considering the absolute value of epoch amplitude, the mean can be calculated using Equation (4.3).

$$Mean, \mu = \frac{1}{N}\sum_{i=1}^{N}|(N\_Pre\_out(i)| \tag{4.3}$$

In the STD calculator block, the mean,μ is determined first. the absolute value of each preprocessed EOG epoch observation is accumulated and divided by the total number of observations to determine the mean,μ. Subtraction of the mean from Pre_out(i) provides deviation. Then, the average of the squared deviation is calculated consecutively using a multiplier, an accumulator, and a divisor circuit. The STD is obtained by the square root of this average squared deviation. The STD_H and STD_V are determined in a serial manner. These values are stored in two registers. Here, the control signal, Ctrl_std(i) maintains the coherency of the operation.

4.3.3 Classification Subsystem

The classification subsystem takes the features as input and decide the output class of eye movement.

Binary Classifier

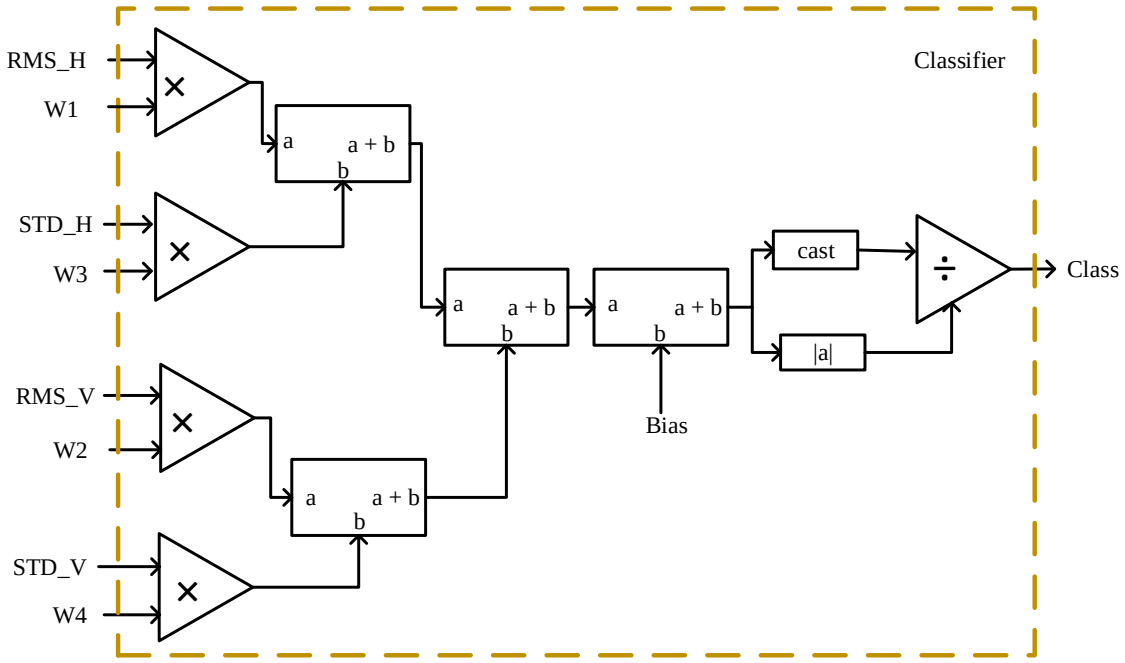


Fig. 4.7 Block diagram of the Binary Classifier

Fig. 4.7 shows the FPGA implementation of SVM classifier. It can be translated

in hardware using Equation (4.4).

$$f(x) = \mathbf{x}'\mathbf{w} + b \tag{4.4}$$

where, **x** contains the features. The vector **w** contains the coefficients or weights that define an orthogonal vector to the hyperplane, and b is the bias term. In this case, **x** contains four features. **w** contains the weights W1-W4 and b is the constant bias. In the classifier block, at first, the features are multiplied by the weights. Then, weighted features are added with bias and results f(x).
Then, the f(x) value is passed through the signum function. The function here simply gives the sign for the given values of f(x) using Equation (4.5).

$$class = \frac{f(x)}{|f(x)|} \tag{4.5}$$

The signum function is realized using a divisor circuit. The output of this classifier subsystem of Figure 4.7 is class. For an f(x) value greater than zero, the value of the class is +1 (blink), and for an f(x) value lesser than zero, the value of the class is -1 (saccade).

Multiclass Classifier

The multiclass classifier subsystem uses a total of five SVM binary classifiers instead of six classifiers to optimize hardware resources. The required circuit for the individual SVM classifier is designed as Fig. 4.7. Five classifiers of similar structures are designed.The output of the five classifiers is combined to provide six class classifications using comparing logic of Algorithm 1 as shown in Fig. 4.8. The Algorithm 1 represents the comparing logic for obtaining the final classified eye movement. It takes C1 - C5 as input and returns 'out' as output. Here, C1 to C5 represent the output of the corresponding classifiers, and out represents the final output of the multiclass classifier. It compares individual classes gradually from class one to five. If class 1 is positive it is decided as the final class. Other-

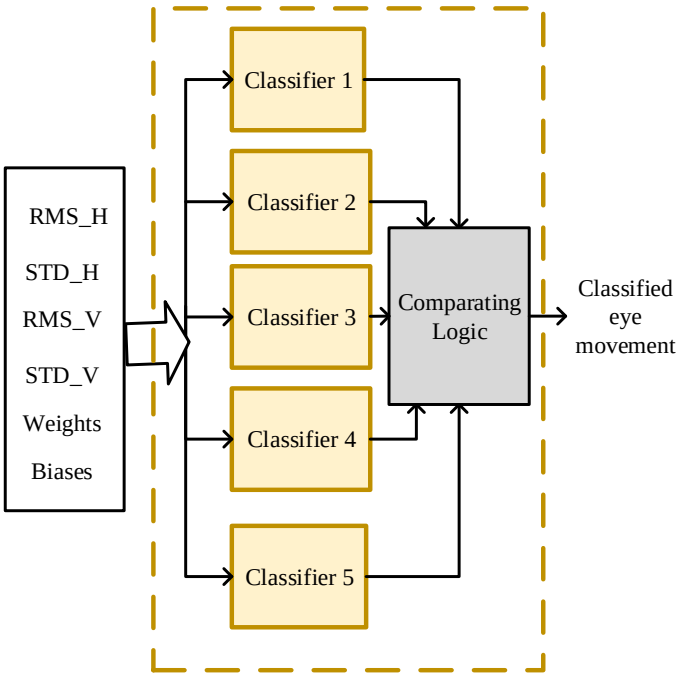


Fig. 4.8 Block Diagram of the Multiclass Classifier

Algorithm 1: The logic of comparator

Input: $C1, C2, C3, C4, C5$
Output: *out*

```
if (C1 = 1) then
    out=1
else
    if (C2 = 1) then
        out=2
    else
        if (C3 = 1) then
            out=3
        else
            if (C4 = 1) then
                out=4
            else
                if (C5 = 1) then
                    out=5
                else
                    out=6
                end if
            end if
        end if
    end if
end if
return out
```

wise, it checks for the next class and so on. Finally, if no class among classes one to five is found true, then it selects class six as output.

4.4 Summary

In this chapter, two compact EOG signal processors are designed. The complete hardware backend for the blink detection and eye movement classification are shown. The designs have taken the hybrid serial-parallel approach to optimize resource utilization and minimize the delay.

Chapter 5: Performance Analysis

This section demonstrates the comparison between the software and hardware results. Then, the resource utilization and power consumption for the implemented prototype are shown. Comparative study with previous studies are also presented.

5.1 Performance analysis of Binary Classification

For evaluating the performance of binary classification, at first, the software hardware output of preprocessing stage, feature extraction stage and classification stage are shown. Then, the power consumption and resource utilization is outlined. Finally, the efficacy is proved with the comparative study.

5.1.1 Results

The magnitude response of the high-pass filter in hardware is shown in Fig. 5.1

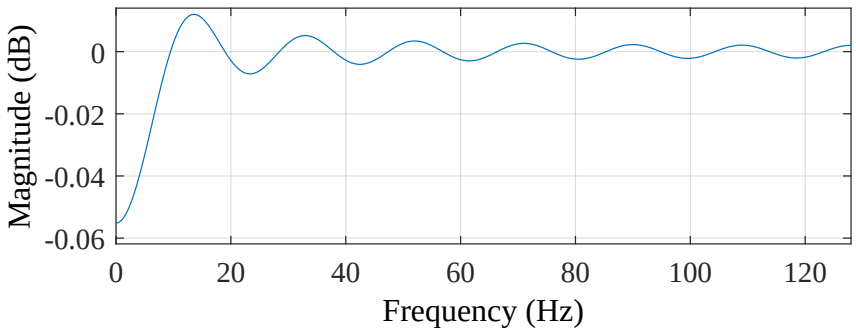


Fig. 5.1 Magnitude Response of High-pass filter in hardware

Here, the obtained cut-off frequency is 0.03 Hz for high-pass filter which is sufficient for baseline wander mitigation [90].

The magnitude response of the low-pass filter in hardware is shown in Fig. 5.2. The obtained cut-off frequency of the low-pass filter is below 30 Hz which is sufficient for further EOG applications [106].

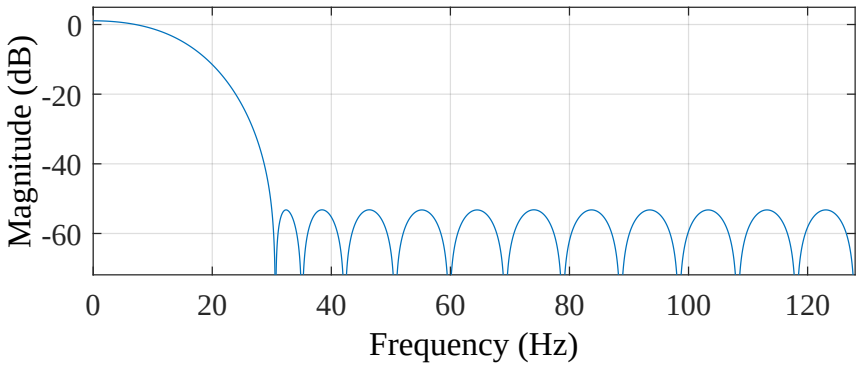


Fig. 5.2 Magnitude Response of Low-pass filter

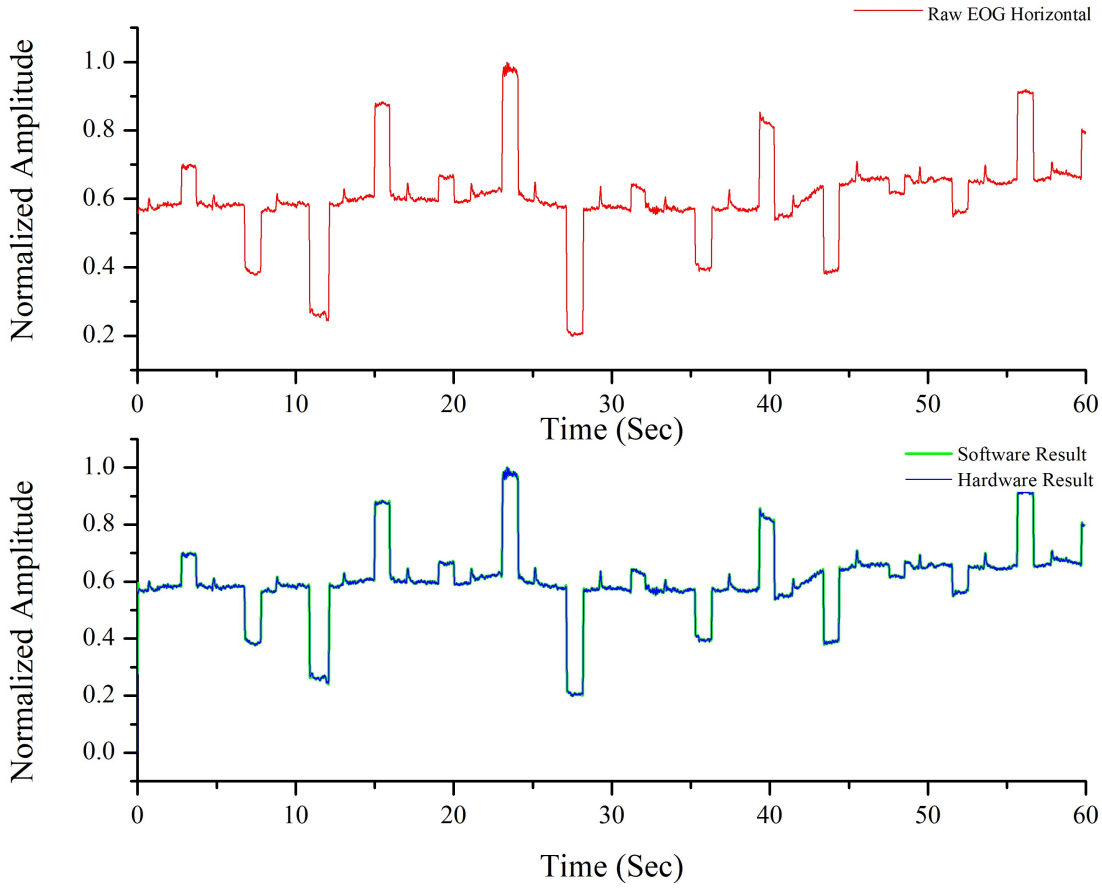


Fig. 5.3 Comparison of raw input and preprocessed Horizontal data

In the preprocessing stage, the software-hardware co-simulation has been performed for 1 min. The designed preprocessor has been tested with 6 subjects. Considering delay of 0.1 sec, input and superimposed software-hardware results for only subject S_1 are shown in Fig 5.3 and 5.4.

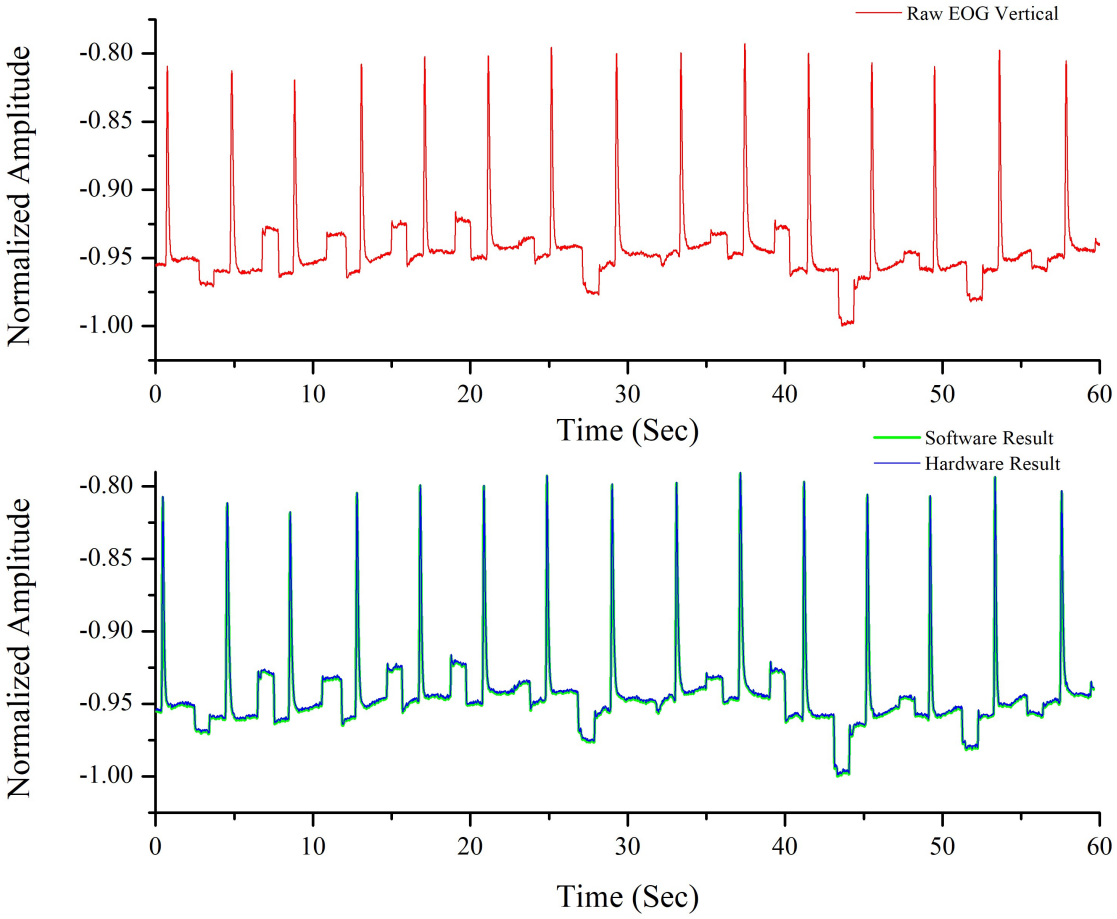


Fig. 5.4 Comparison of raw input and preprocessed Vertical Data

The frequency response of input and preprocessed output of both software and hardware output for the same subject are shown in Fig. 5.5 and 5.6.

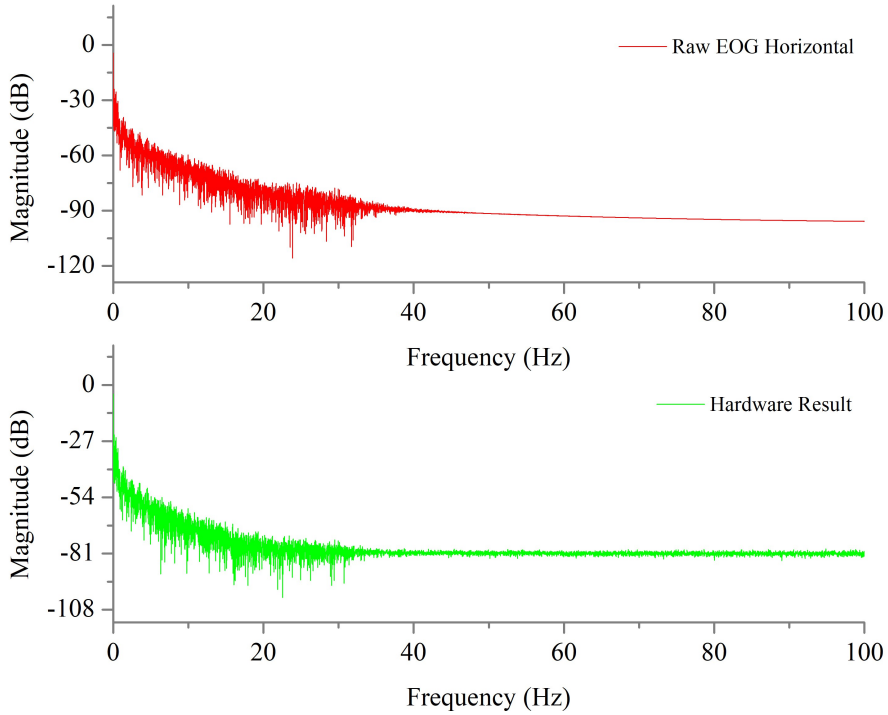


Fig. 5.5 Comparison of the frequency response of input and hardware output for Horizontal Data

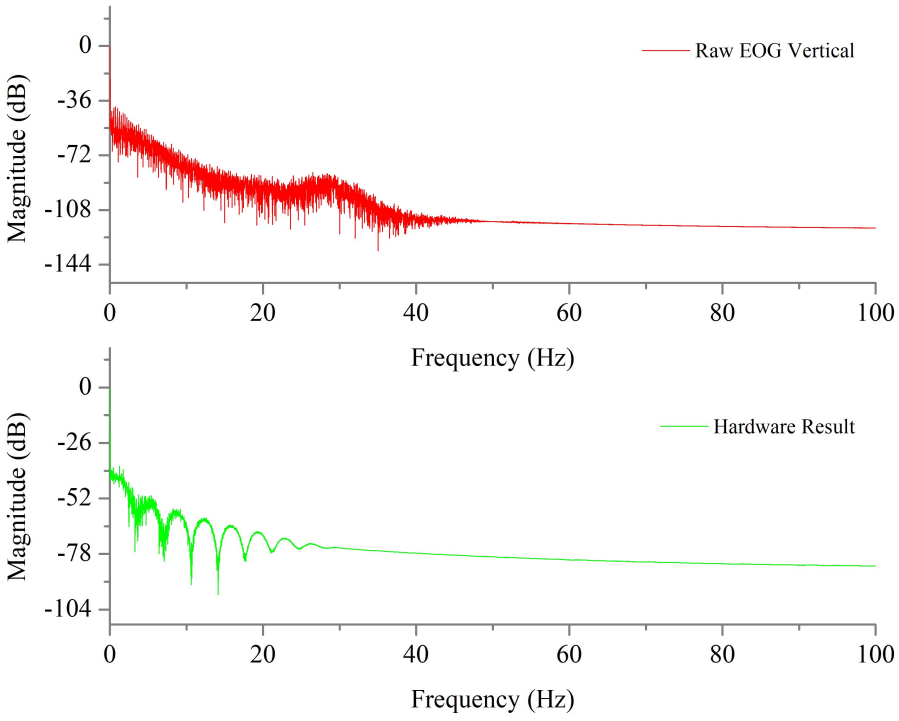


Fig. 5.6 Comparison of the frequency response of input and hardware output for Vertical Data

For further statistical comparison, correlation and root squared error (RSE)[102] between the hardware-software outputs are calculated. Correlation is found from

the Pearson Correlation Coefficient, r as given in (5.1). Then, RSE is calculated as given in (5.2).

$$r = \frac{1}{n-1}\left(\frac{\sum_X \sum_Y (X-\overline{X})(Y-\overline{Y})}{S_X S_Y}\right) \tag{5.1}$$

$$RSE = \sqrt{(X-Y)^2} \tag{5.2}$$

Here, n denotes the total number of paired data. X and Y are the simulation and hardware outputs respectively. The averages of these corresponding data are presented by $\overline{X}$ and $\overline{Y}$ respectively. S_X and S_Y denote the corresponding standard deviations.

Table 5.1: The Pearson Correlation Coefficient in preprocessing stage of Binary Classification

Subjects	**Horizontal Data**	**Vertical Data**
S_1	0.9991	0.9847
S_2	0.9973	0.9873
S_3	0.9997	0.9911
S_4	0.9962	0.9927
S_5	0.9982	0.9919
S_6	0.9996	0.9921
Average	0.9984	0.99

Table 5.1 represents the pearson correlation coefficients for 6 subjects. For this design, all the median values are higher than 0.99. On average, r = 0.9984 for horizontal EOG and r = 0.99 for vertical EOG. Generally, this coefficient stays within 0 to 1. Closeness of this parameter to 1 means better correlation i.e. higher accuracy. So, a remarkable agreement is ensured between the software model and designed FPGA hardware model.

The RSE between software-hardware results for horizontal and vertical EOG are calculated to show the agreement of the model with hardware-software codesign.

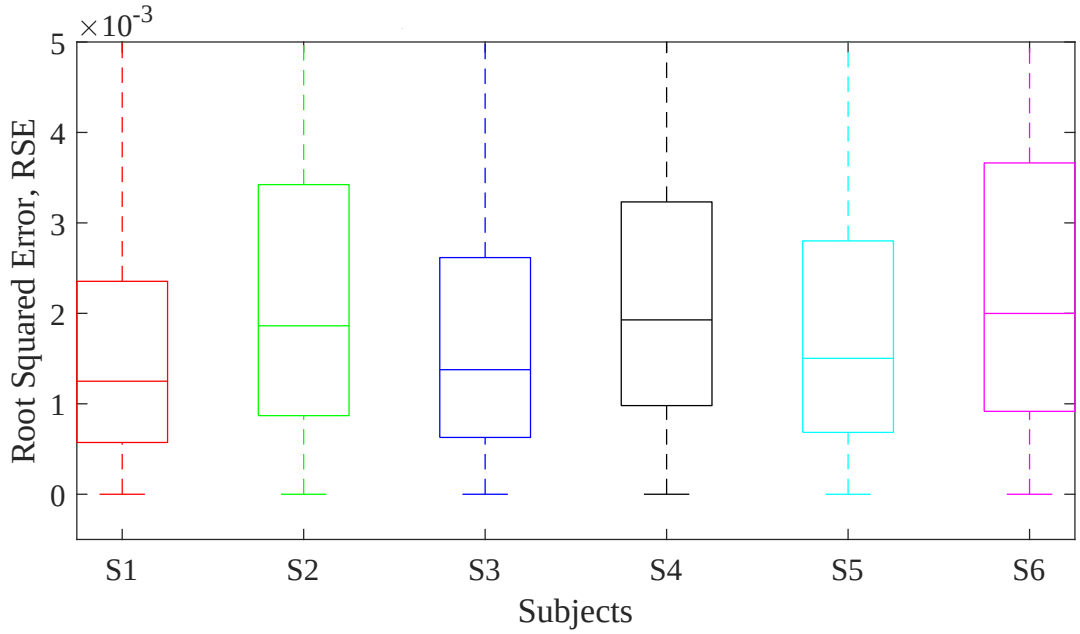


Fig. 5.7 RSE of preprocessed horizontal EOG data

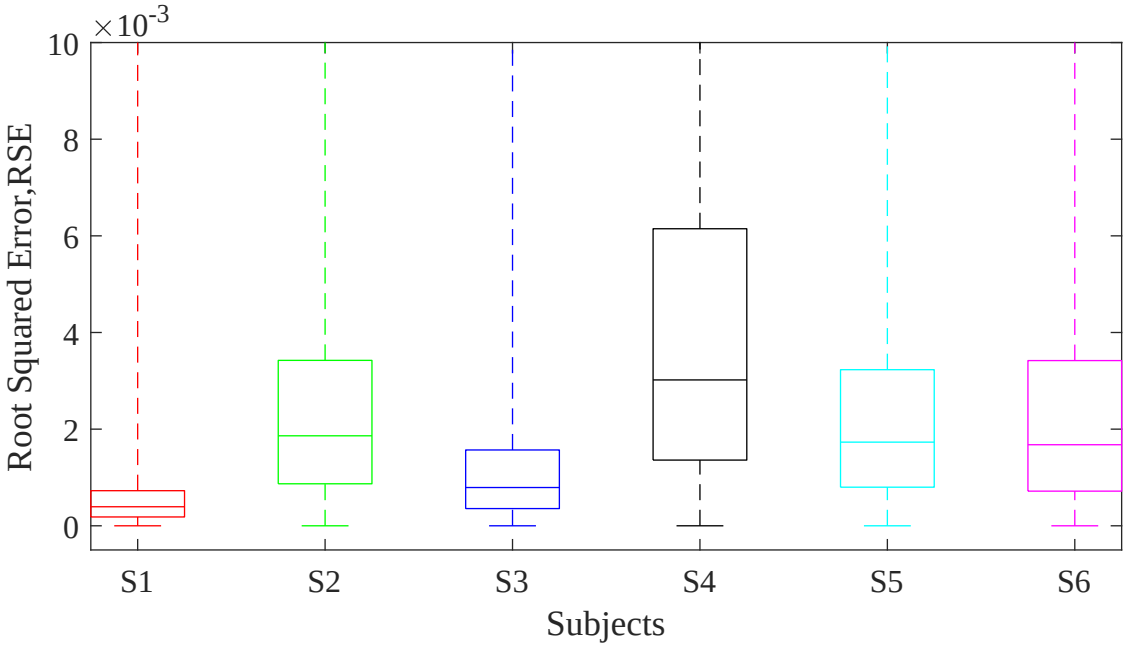


Fig. 5.8 RSE of preprocessed vertical EOG data

Boxplots of Fig.5.7 and Fig. 5.8 show the RSE for horizontal EOG signal and Vertical EOG signal respectively. Here, mean RSE values for all six subjects are in the 10^{-3} range. These values are close to 0. Therefore, the hardware model is further validated.

Fig. 5.9 depicts the confusion matrix of the binary classifier. The number of true positive (TP), false positive (FP), true negative (TN), and false negative (FN) cases are 744, 27, 309, and 0 respectively.

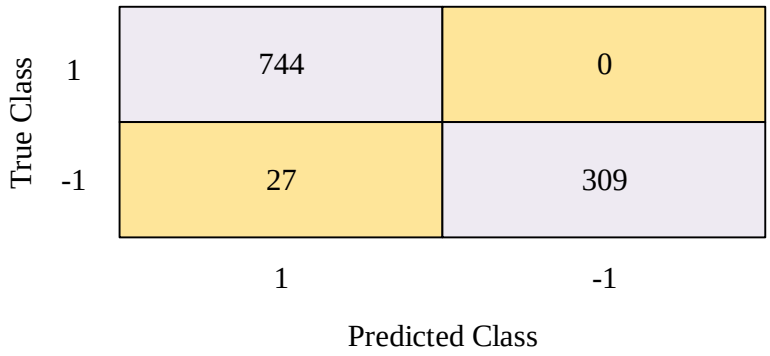


Fig. 5.9 Confusion matrix for binary classification in software

Here, TP represents the cases where blink is detected as blink, FN represents the cases where the blink is detected as saccade, TN represents the cases where saccade is detected as saccade, and FP represents the cases where Saccade is detected as blink. A number of parameters such as accuracy, precision, recall, and F1 score are calculated to verify and analyze the system performance of the proposed classifier.

Accuracy is a measurement statistic that compares the proportion of accurate predictions made by a model to total predictions. It can be determined by Equation (5.3).

$$Accuracy = \frac{TN + TP}{TN + TP + FN + FP} * 100 \tag{5.3}$$

Sensitivity means how well a machine learning model can identify positive examples. It is also known as Recall. It can be expressed by Equation (5.4).

$$Sensitivity = \frac{TP}{TP + FN} * 100 \tag{5.4}$$

Specificity refers to how an algorithm or model can forecast a true negative for each possible category. It is defined by Equation (5.5).

$$Specificity = \frac{TN}{TN + FP} * 100 \tag{5.5}$$

Precision represents the quality of a positive prediction made by the mode It is defined by Equation (5.6).

$$Precision = \frac{TP}{TP + FP} * 100 \tag{5.6}$$

The F1 score can be calculated as the harmonic mean of the precision and recall scores as given in Equation (5.7).

$$F1\ score = \frac{TP}{TP + 0.5 * (FP + FN)} * 100 \tag{5.7}$$

The accuracy, sensitivity, specificity, precision, and F1 score for software design are 97.5%, 100%, 91.64%, 96.5%, and 98.22% respectively.

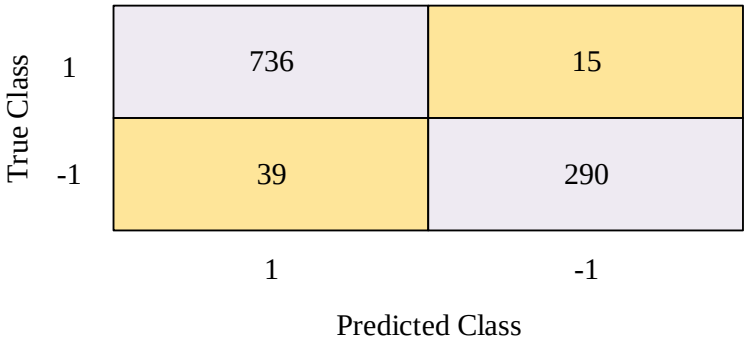


Fig. 5.10 Confusion matrix for binary classification in hardware

The proposed model is implemented on Xilinx Artix-7 FPGA. The accuracy of the implemented EOG processor is 95% using the confusion matrix shown in Fig. 5.10. Verification of the classifier stage is done by the software-hardware agreement. Therefore, root mean square and the Pearson correlation coefficient are calculated [102]. The root mean square value is found in 10^{-3} range and the Pearson correlation coefficient is 0.98. These values represent that the hardware design for binary classification agrees with the software model.

Table 5.2 shows the FPGA resource utilization for this design. Usage of Look Up Table (LUT), LUT-Random-Access Memory (LUTRAM), Flip-Flops (FF), Blocked Random-Access Memory (BRAM), Digital Signal Processing (DSP), Bonded In-

Table 5.2: FPGA resource utilization in ZedBoard for binary classification

Resource	Utilization	Available	Percentage Utilization
LUT	19684	53200	37%
LUTRAM	696	17400	4%
FF	4256	106400	4%
BRAM	1	140	1%
DSP	119	220	54%
IO	92	200	46%
BUFG	1	32	3%

Table 5.3: FPGA power consumption in Zedboard for binary classification

	Logic Operation	Power Consumption
Dynamic (86%)	Clocks	0.029 W (4%)
	Signals	0.306 W (45%)
	Logic	0.241 W (35%)
	BRAM	0.007 W (1%)
	DSP	0.076 W (11%)
	IO	0.025 W (4%)
Device Static (14%)	PL Static	0.0116 W
Total On-Chip power		**0.8 W**

put/Output blocks (IO) and Global Buffer (BUFG) are 37%, 4%, 4%, 1%, 54%, 46%, and 3% respectively.

Power consumption in Zedboard consists of major two components. These are static power, P_S and dynamic power, P_D [107].

Static power or standby power refers to the total amount of power the device consumes when it is powered up but not actively performing any operation. This is caused mainly by the leakage current between power supply and ground.

Dynamic power or active power refers to the total amount of power the device consumes when it is actively operating. The dynamic power mainly causes due to signal transitions happening in the transistors [108]. The dynamic power consumption can be expressed as the following equation.

$$P_D = \sum_i C_i^2 . V_i . f_i \tag{5.8}$$

Here, C_i , V_i , and f_i refer to capacitance, the voltage swing, and clock frequency

of the resource *i*, respectively. It can be said that, the summation of the dynamic power of each resource leads to the total dynamic power. FPGA allows flexibility in programming. Hence, the individual designs affect the dynamic power.
As shown in Table 5.3 the designed prototype uses a total of 0.8 W power only. Dynamic power consumption of 0.684 W (86%) is utilized in Clocks (0.029 W), Signals (0.306 W), Logic (0.241W), BRAM (0.007W), DSP (0.076W), and I/O (0.025 W). The static power consumption is 0.116 watts (14%).

5.1.2 Comparative Study

Table 5.4 compares this work and state-of-the-art works of EOG based blink detection. Banerjee et al. [88] achieved 95.33% accuracy in blink detection with RBF kernel SVM. Ryu et al. [24] achieved 94.3% accuracy in detecting blinks, horizontal saccades, vertical saccades, and fixation with differential EOG signal based on a fixation curve (DOSbFC) method for baseline drift and noise removal. Molina-Cantero et al. [17] achieved 89.9% accuracy with adaptive K-means for classifying single blink, double blink, and long blink. Gundugonti and Narayanam used thresholding for blink and saccade detection and implemented in FPGA [89].
The proposed design has better accuracy than all state-of-the-art works. This work demonstrates a machine learning based ASIC implementation of EOG processor incorporating preprocessing, feature extraction, and classification stages for blink detection.

Table 5.4: Comparative study of state-of-the-art works of EOG based blink detection

References	**Detection Approach**	**Accuracy**	**Implementation**			**Device**
			Preprocessing	Feature Extraction	Classification	
Banerjee et al. [88]	RBF kernel SVM	95.33%	×	×	×	×
Ryu et al. [24]	DOSbFC and Thresholding	94.3%	×	×	×	×
Molina-Cantero et al. [17]	Adaptive K-means	89.9%	✓	×	×	Discrete
Gundugonti and Narayanam [89]	DWT and Thresholding	-	✓	×	✓	FPGA
This work	Linear SVM	97.5%* and 95%**	✓	✓	✓	FPGA

*Software Accuracy, **Hardware Accuracy

5.2 Performance analysis of Multiclass Classification

In this section, the performance of the designed EOG processor for the multiclass classification is evaluated. Results from the software system and hardware system are shown. Then, the hardware resource utilization and power consumption will be discussed, and finally, a comparative study will be presented to validate the efficacy of the designed system.

5.2.1 Results

The raw data is preprocessed using filters in preprocessing stage. Fig. 5.11 and Fig. 5.12 shows magnitude response of the high pass and low pass filters respectively.

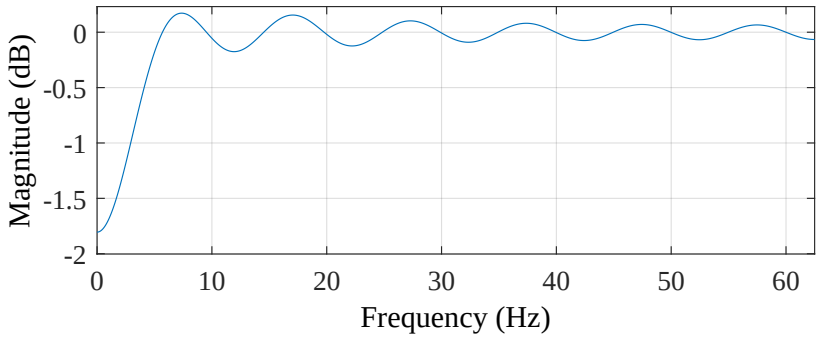


Fig. 5.11 Manitude response of high pass filter

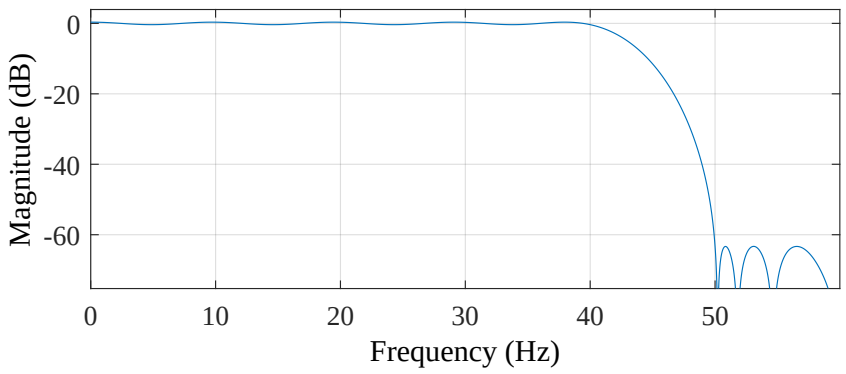
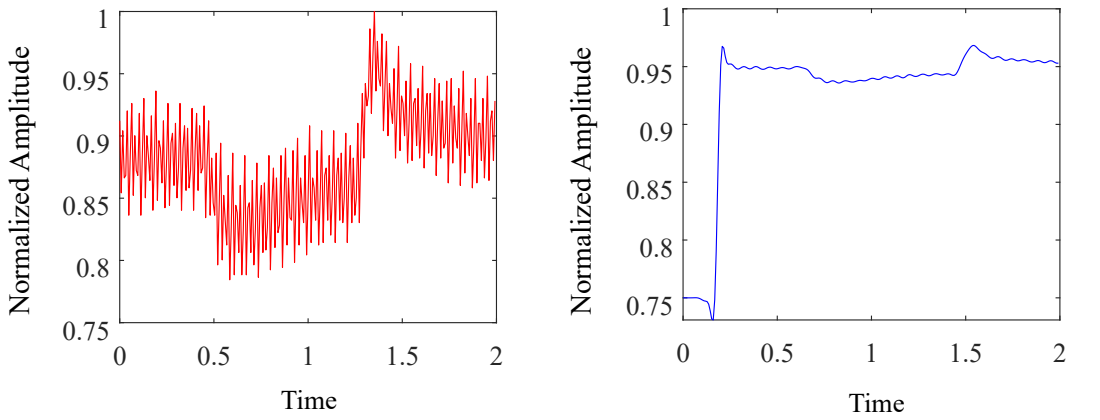


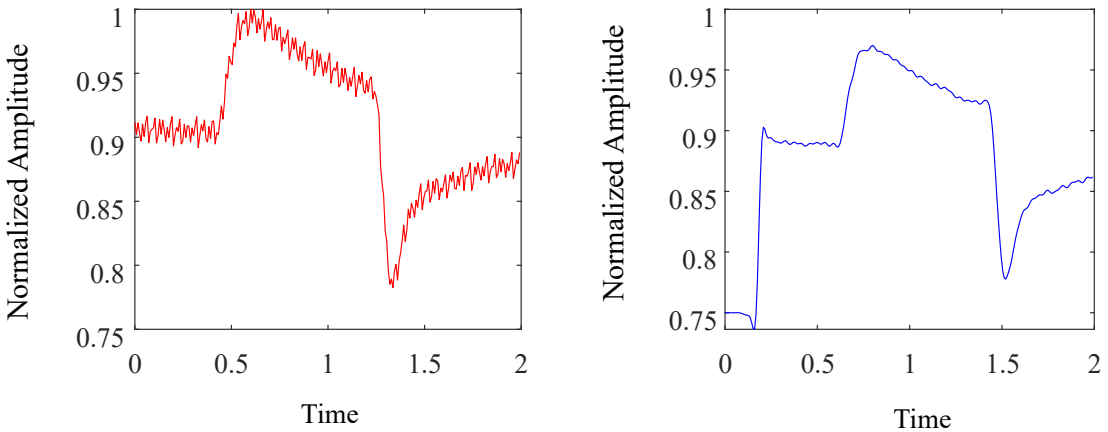
Fig. 5.12 Manitude response of low pass filter

Fig. 5.13 shows raw input and preprocessed output of horizontal EOG signal. Fig. 5.14 shows raw input and preprocessed output of vertical EOG signal.



a) Raw horizontal EOG signal b) Preprocessed horizontal EOG signal

Fig. 5.13 Raw and preprocessed horizontal EOG signal



a) Raw vertical EOG signal b) Preprocessed vertical EOG signal

Fig. 5.14 Raw and preprocessed vertical EOG signal

The correlation coefficient value is calculated considering the associated delay in hardware after the preprocessing stage. The dissimilarities in the figures of raw and preprocessed signals are due to the delay added in the hardware after filtering. However, they maintain high correlation coefficients.The Pearson corelation coefficient between the software and hardware results after preprocessing

stage for all subjects is shown in Table 5.5. The average value lies around 0.97. This proves the software hardware agreement of the design.

Table 5.5: The Pearson Correlation Coefficient in preprocessing stage of Multiclass Classification

Subjects	**Horizontal Data**	**Vertical Data**
S_1	0.9891	0.9973
S_2	0.9493	0.9873
S_3	0.9972	0.9411
S_4	0.9762	0.9327
S_5	0.9524	0.9614
S_6	0.9796	0.9421
S_7	0.9897	0.9737
S_8	0.9672	0.9877
S_9	0.9872	0.9719
S_{10}	0.9897	0.9721
Average	0.9777	0.9667

After preprocessing stage, features are extracted from the preprocessed signals. Fig. 5.15 represents total of four features: RMS value of horizontal EOG signal (RMS_H), STD value of horizontal EOG signal (STD_H), RMS value of vertical EOG signal (RMS_V), and STD value of vertical EOG signal (STD_V) used in this work. Here, epochs 1-100 represent no movements, samples 101-200 represent down movement, epochs 201-300 represent left movements, epochs 301-400 represent blink, and epochs 401-500 represent right movement, and epochs 501-600 represent up movement.

The Root Squared Error, and the Pearson Correlation Coefficient are calculated to check the hardware and software agreement. Fig. 5.16 shows the boxplot of corresponding root squared errors, all notably close to 0. This supports the validity of the hardware design. The correlation coefficient for all categories varies between 0 to 1. A value closer to 1 indicates a higher accuracy. In this work, all the median values are greater than 0.91 indicating a significant agreement between

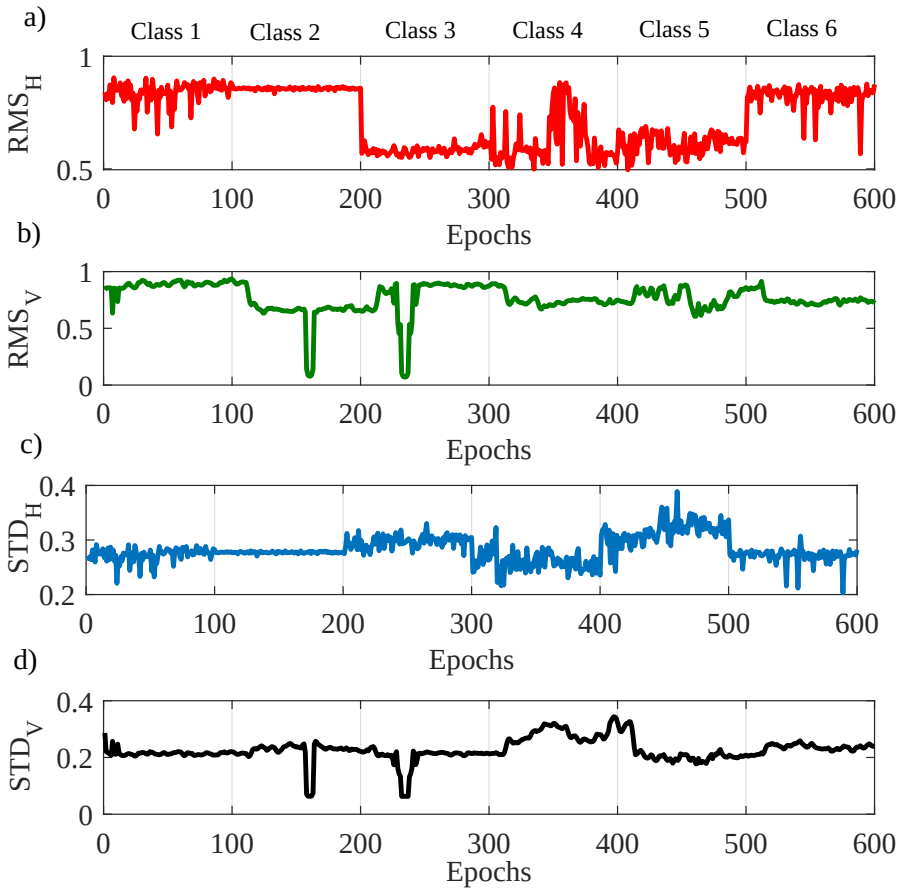


Fig. 5.15 Features of EOG signals (a) RMS of EOG_h, (b) RMS of EOG_v, (c) STD of EOG_h,and (d) STD of EOG_v

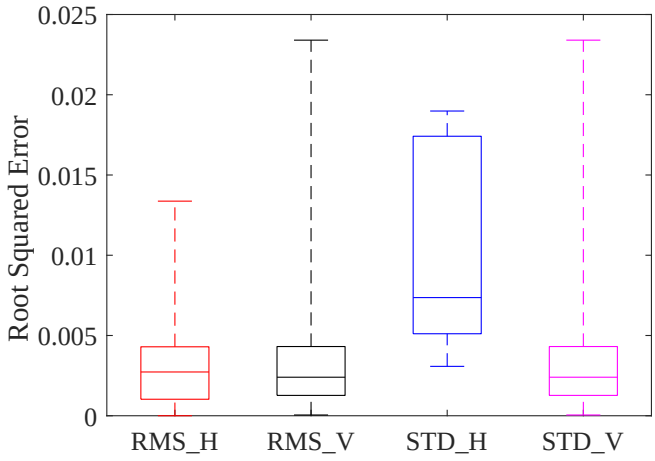


Fig. 5.16 Root Squared Error between software and hardware outputs in feature extraction stage

the software and hardware models.

In this design, six classes are considered for multiclass classification. The classifier is developed based on the SVM classifier. The comparator output gives the

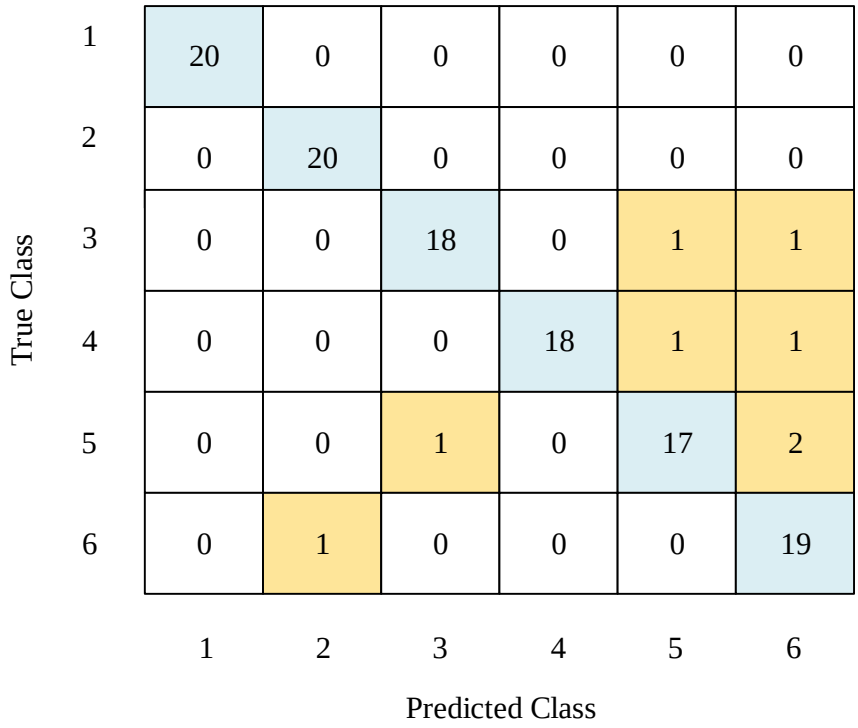


Fig. 5.17 Confusion matrix for multiclass classification in software

final result to detect the eye movement class. The dataset is split into 80:20 ratios for training and testing. The confusion matrix for this classifier is shown in Fig. 5.17. The true positive predictions are marked in blue and wrong predictions are marked in gold. Here, class 1 represents no movement, class 2 represents down movement, class 3 represents left movement, class 4 represents blink, class 5 represents right movement, class 6 represents up movement. Among the different classes, the developed system can predict all the 20 no movement and 20 down movement test data accurately. In the case of left eye movement, it can predict 18 test data accurately. For blink and right movements, the correct predicted test data are 18, and 17 respectively. The designed model can detect 19 up eye movement data correctly.

There are various factors that contribute to a range of levels of accuracy in different eye movements, including highlighted elements, learning context, complex background, low relevance of images and texts, learner differences, awareness of experimental settings, self-conception, and prior knowledge [116]. Individual software accuracy for the above-mentioned six classes is listed in Table 5.6. The

average software accuracy is found 97.52%. The accuracy, sensitivity, specificity, precision, and F1-score of all classes are summarized in Table 5.6.

Table 5.6: Performance analysis of Multiclass classifier

Movement	Accuracy	Sensitivity	Specificity	Precision	F1-score
No movement	100%	100%	100%	100%	100%
Down	100%	100%	100%	100%	100%
Left	97.5%	90%	98.01%	94.73%	92.30%
Blink	98.33%	90%	98.03%	100%	94.73%
Right	95.83%	85%	97.02%	89.47%	87.17%
Up	95.83%	95%	98.96%	82.60%	88.37%
Average	97.92%	93.33%	98.67%	94.47%	93.76%

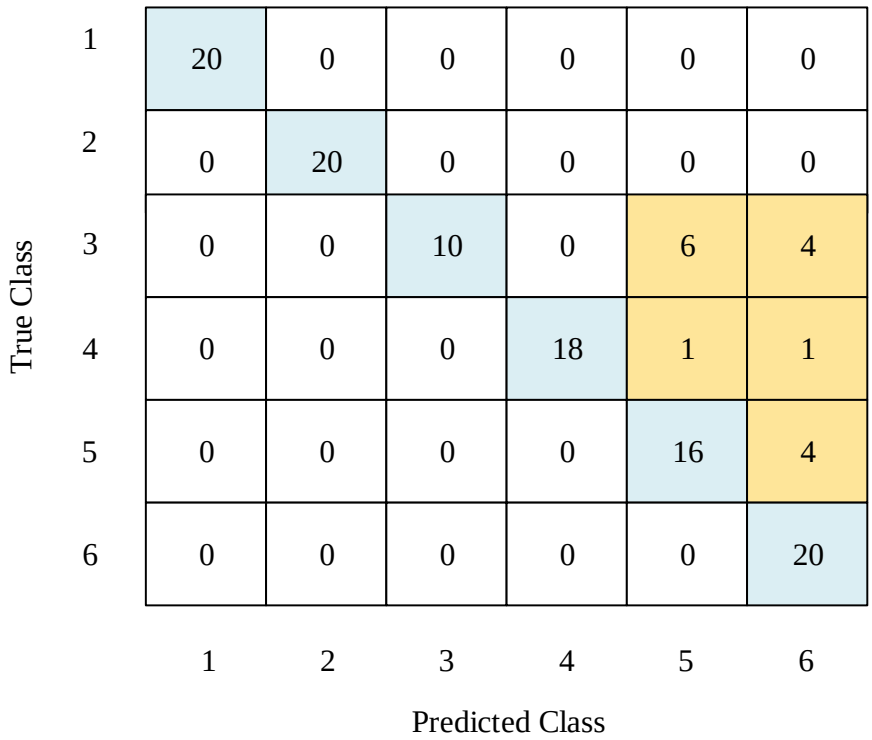


Fig. 5.18 Confusion matrix for multiclass classification in hardware.

The designed EOG processor is implemented in Zynq UltraScale+ ZCU106. Fig. 5.18 shows the confusion matrix for the hardware classifier. The confusion matrix of software and hardware shows differences. The possible reasons can be precision and memory constraints in hardware. The real-time data is floating

type. Hardware implementations use fixed-point for reduced precision arithmetic while calculations are performed. This leads to loss of information and rounding errors. This may affect the accuracy of the model, especially for class 3. Additionally, hardware-implemented systems face the issue of limited memory resources compared to software implementations. In the case of class 3, the model or data size may exceed these limits, which may lead to reduced accuracy. The individual classes' accuracies for the proposed design's SVM classifier are listed in Table 5.7. The average accuracy for six classes is 95.56%.

Table 5.7: Comparison of testing accuracy of multiclass classifier in software and hardware

Movement	**Software accuracy**	**Hardware accuracy**
No movement	100%	100%
Down	100%	100%
Left	97.5%	91.67%
Blink	98.83%	98.33%
Right	95.83%	90.83%
Up	95.83%	92.5%
Average	97.92%	95.56%

Table 5.8: FPGA resource utilization in Zynq UltraScale+ for multiclass classification.

Resource	**Utilization**	**Available**	**Percentage Utilization**
LUT	40207	230400	17.45%
LUTRAM	736	101760	0.72%
FF	7657	460800	1.66%
BRAM	2	312	0.64%
DSP	232	1782	13.43%
IO	75	360	20.83%
BUFG	1	544	0.18%

Table 5.8 presents hardware resource utilization for the prototype. Here, LUT, LUTRAM, FF, BRAM, DSP, IO, and BUFG denote Look Up Table, LUT-Random-Access Memory, Flip-Flops, Blocked Random-Access Memory, Digital Signal Pro-

cessing, Bonded Input/Output blocks,and Global Buffer respectively. The design utilizes 17.45% LUT, 0.72% LUTRAM, 1.66% FF, 0.64% BRAM, 13.43% DSP, 20.83% IO, and 0.18% BUFG. Total system delay associated in this design is 18.4 μs only, which is inherently introduced by the FIR filter of preprocessing unit [117].

The on-chip power consumption in Zynq Ultrascale+ FPGA for this design is 1.446 watts. The power is consumed as dynamic power and static power. The total consumption of dynamic power is 0.850 watts (59%) and static power is 0.596 watts (41%). Dynamic power is utilized in Clocks (0.033 W), Signals (0.374W), Logic (0.336W), BRAM (0.004W), DSP(0.102W), and I/O (0.001 W) as shown in Table 5.9. Static power is utilized in PL static (0.583 W) and PS static (0.013W).

Table 5.9: FPGA power consumption in Zynq UltraScale+. for multiclass classification

	Logic Operation	**Power Consumption**
Dynamic (59%)	Clocks	0.033 W (4%)
	Signals	0.374 W (44%)
	Logic	0.336 W (40%)
	BRAM	0.004 W (1%)
	DSP	0.102 W (11%)
	IO	0.001 W (0%)
Device Static (41%)	PL Static	0.583 W (98%)
	PS Static	0.013 W (2%)
Total On-Chip power		**1.446 W**

5.2.2 Comparative Study

Table 5.10 summarizes a comparative study between this work and state-of-the-art reconfigurable EOG eye movement classification techniques. J. F. Wu et al. [79] implemented preprocessing and classification stages. Cano et.al [67] and Asanza et. al [13] implemented only the classification stages. The proposed work shows higher accuracy than all previous works. To the best of my knowledge, this is the first work incorporating hardware implementation of all processing stages for EOG. Thus this work provides a complete EOG processor to classify eye movements.

Table 5.10: Comparative study of machine learning based EOG reconfigurable implementation

References	Hardware Implemented Stage			No. of Features	Classification Techniques	No. of Classes	Accuracy
	Preprocessing	Feature Extraction	Classification				
J. F. Wu et al. [79]	✓	×	✓	3	Linear SVM	4	92.30%
Cano et al.[67]	×	×	✓	-	CNN	3	65%
Asanza et al. [13]	×	×	✓	4	Cuvic SVM	6	93.50%
This work	✓	✓	✓	4	Linear SVM	6	*97.92% , and **95.56%

*Software Accuracy, **Hardware Accuracy

5.3 Summary

In this chapter, the results and performance of the designed systems are shown. The first design detects the saccades and blinks efficiently with software and hardware accuracies of 97.5% and 95% respectively. The on-chip power consumption for this design is only 0.8 watts. Experimental results demonstrate the efficacy of the designed EOG processor in terms of classification accuracy, implementation complexity, and power consumption. Then, the design of the EOG signal processor for multiclass classification is evaluated. It classify six different movements of eyes- No Movement, Down, Left, Blink, Right, and Up from Dual channel EOG Signals. The software design provides 97.92% accuracy using only two features. The implemented prototype offers 95.56% accuracy. It uses a total of 1.446 watts of on-chip power. Experimental results and comparative studies demonstrate the efficacy of the designed EOG processor.

Chapter 6: Conclusions

Eye diseases are one of the major contributors to disabling conditions. These diseases can ultimately turn severe and can lead to blindness. Eye movement analysis can work as a key factor in the diagnosis of eye diseases. Electrooculoculography is one of the suitable techniques to provide eye movement information through electrooculogram (EOG) signal. The reasons are: EOG signal acquisition is cheap, non-invasive, and presents almost no adverse health effects. Implementing machine learning algorithms with traditional signal processing techniques is opening new domains in the EOG research field. Hence, EOG signal analysis is now widely used in human-machine interfaces, wheelchair control, sleep stage study, etc. However, high-performance dual-channel EOG processing needs fast computation. Conventional microprocessors can face burdens in computing during real-time EOG siganl processing. FPGA-based reconfigurable architecture presents the perfect solution for time-critical energy-efficient dual-channel EOG signals. An in-depth analysis of the software backend and hardware implementation of two novel FPGA-based EOG signal processors is discussed throughout this thesis. In this final chapter, the contribution and significance of this research work are summed up. At first, an overview of the work is presented by giving a summary of the designed prototypes and key findings. This chapter ends by mentioning the limitations of this research along with a few potential future research opportunities.

6.1 General Summary

EOG is an electrophysiological signal that provides insights into eye movements. The eye movement detected from the EOG signals can be very useful in human-machine interface applications and in detecting diseases that are related to eye movements. This work provides a systematic review of EOG point-of-care sys-

tems based on EOG hardware implementations. Two novel research works are described in the previous chapters of this thesis. These works give insights and jointly advance the development of eye movement detectors using machine learning approaches. The software framework behind the proposed methods is presented, leading to optimized hardware implementation using FPGA. In short, this research utilized the advantages of reconfigurable architectures to develop high-performance domain-specific processors for EOG signal processing.

6.2 Key Findings

The key findings of this thesis can be outlined as:

- A systematic review is done for Electrooculogram (EOG) Point of care (POC) systems. It includes all hardware implementations of classifications work solely done on EOG signals in the last five years. The present scenario of data acquisition techniques, preprocessing techniques, features used, and various algorithms for EOG processing are outlined. This review finds the research gap for the development of POC systems solely using EOG. To the best of my knowledge, this is the first systematic review work of EOG based POC systems.

- An application-specific EOG processor intended to detect blinks is designed. The EOG signals are preprocessed using FIR filters of minimum order. Statistical features are extracted and then used for classification. The designed architecture detects the saccades and blinks efficiently with software and hardware accuracies of 97.5%. As the aim of this thesis, the software backend design is used to implement a hardware-based system for detecting the blinks. FPGA is chosen for its advantage over other hardware-based platforms. Xilinx system generator has been used for the design procedure and Zedboard zynq 7000 board has been employed primarily for implementation. The implemented prototype shows 95% accuracy. Hardware resource

utilization for different units and power consumption are presented. The on-chip power consumption for this design is only 0.8 watts. Experimental results demonstrate the designed EOG processor offers intended characteristics in terms of classification accuracy, implementation complexity, and power consumption. The comparative study confirmed the efficacy of the designed EOG processor for blink detection using a binary SVM classifier. The achieved results shows better accuracy than state-of-the-art hardware implemented blink detectors.

- A proof-of-concept complete digital system to classify six different eye movements (up, down, normal, right, left, and blink) is designed. The prototype design utilizes a combination of serial-parallel techniques for hardware optimization. This design achieves an average software accuracy of 97.92%. Zynq Ultrascale+ FPGA board has been employed for the multiclass classification of eye movements. The implemented design offers 95.56% accuracy utilizing the SVM classifier. The statistical analysis proves the software-hardware agreement. Experimental results show that the hardware system offers satisfactory classification accuracy, and power consumption performance. The comparative study confirmed the efficacy of the designed EOG processor for six different eye movements using a multiclass SVM classifier. To the best of my knowledge, there is no previous machine learning-based compact EOG processor that includes all machine learning stages to classify six class eye movements. Therefore, it is the first of its kind in this regard.

Although these works have their stand-alone characteristics, they ultimately work towards the common goal of developing domain-specific EOG signal processors using reconfigurable computation.

6.3 Limitation of the study

There are a few limitations of this work. They are mentioned below.

- The accuracy of the blink detector and eye movement detector can be improved further.
- The Binary classification design uses 0.8 W and the hardware design uses 1.446 W. To intrgrate this proof-of-concept designs in HMI application power consumption needs to be reduced.

6.4 Future Research Directions and Opportunities

The designed systems can be utilized and improved for future studies. There are scopes to develop wearable devices, wheelchair controls, smart healthcare systems, security systems, and point-of-care systems using FPGA-based designs. There is a scope for research in each stage of the processor design, preprocessing, feature extraction, and classification; especially for extracting hardware-friendly features. Proper selection of preprocessors, features, and classifiers can optimize the resources and associated costs.

The eye movement classification approaches of this work can be utilized to identify the two most common forms of abnormal eye movements termed nystagmus and strabismus. Nystagmus refers to an eye disease when both eyes move together in short erratic patterns. Strabismus is a disorder that results in misaligned eye movements due to poor eye-muscle coordination. Further research is needed to ensure the integration of compact EOG processors into clinical diagnostics, wheelchair control, smart cars, IOT-based systems, and security systems. One FPGA chip can be programmed for multiple signal-processing tasks as it provides reconfigurable architecture. VLSI realizations of the FPGA-based prototypes can result in a future reduction of hardware complexity and power consumption.

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Appendices

Appendix A: Description of the Dataset

Eye Movement EOG Data is used for binary classification in this work. A brief description of the dataset is given below.

1. Experimental Paradigm

   This dataset comprises electrooculography (EOG) data recorded from six healthy participants (2 males and 4 females; mean age 24.7 3.1 years), having normal or corrected-to- normal vision. The adopted eye movement data acquisition protocol was approved by the University Research Ethics Committee (UREC) at the University of Malta and before each recording session, each subject provided their informed consent. Subjects were seated 60 cm away from a 24-inch LCD monitor, with their head held immobile using an ophthalmic chin and forehead rests.

   Subjects were asked to fixate their point of gaze (POG) on a highlighted cue on the screen. Specifically, a number of 4 s trials as shown in Fig. A1 were recorded, wherein the subject was asked to perform a saccade originating from the centre of the screen to a random target location in the first 1 s. This was followed by the corresponding return movement towards the centre of the screen in the next 1 s, and a blink in the last 2 s of each trial. A total of 300 such trials were recorded for each subject, in three separate sessions, specifically with 100 trials being recorded in each session. Intermittent breaks were provided in between sessions.

   The corresponding eye movements were recorded using a standard EOG setup. The electrode configuration adopted is shown in Figure A2 where two electrodes were placed adjacent to the lateral canthi while another pair

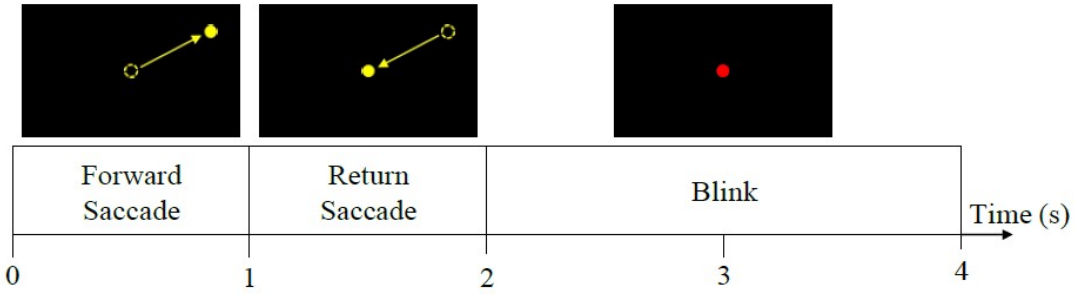


Fig. A1 Timing scheme of one trial

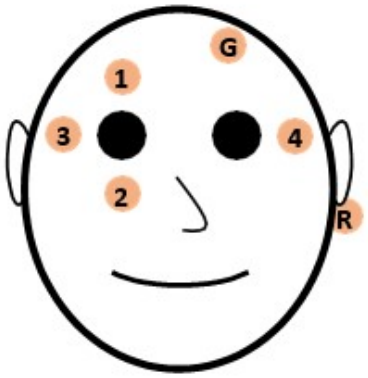


Fig. A2 EOG Electrode configuration of Dataset 1

was placed above and under the right eye, as shown. A ground ('G') and a reference ('R') electrode were also attached on the forehead and on the mastoid behind the left ear respectively. The EOG signals were recorded using the g.tec g.USBamp bio-signal amplifier (g.tec medical engineering GmbH, Austria) with a sampling frequency, Fs = 256 Hz. The recorded data was filtered using a bandpass filter between 0-30 Hz and a 50 Hz notch filter. The EOG potential differences between the horizontally-aligned and vertically-aligned electrodes were then computed to yield what is generally referred to as the horizontal and vertical EOG signal components respectively. $EOG_h(t)$ and $EOG_v(t)$ respectively.

2. Data Format The data is provided in MATLAB (*.mat) format. The data recorded for each subject X is provided in separate folders named SX. In each folder, the following files are provided:

   - EOG.mat: This stores the recorded horizontal and vertical EOG com-

ponent data. Specifically, the first row comprises the horizontal EOG component, whereas the second row comprises the vertical EOG component.

- ControlSignal.mat: This file stores a control signal, of the same size as EOG.mat, where each sample contains a value, '1', '2' or '3', which identifies whether that particular sample corresponds to a forward saccade ('1'), return saccade ('2') or blink ('3').
- TargetAngles.mat: This file contains the horizontal (1st column) and vertical (2nd column) absolute target gaze angles for each saccade, in degrees.

Electromyography of the Extraocular Muscles (EOM) dataset is used for multiclass classification in this work. A brief description of the dataset is given below.

1. Experimental Paradigm

   The electrodes are sensors capable of reading EMG signals or ocular myoelectric activity during eye movements. For this purpose, two vertical electrodes and two horizontal electrodes were used, with a reference electrode on the forehead as shown in Fig. A3. 10 subjects performed 10 pseudorandom repetitions of each of the following eye movements during the experiment: Up, Down, Right, Left, no movement (fixation in the center), and blinking.

   The signal captured by the electrodes passes to an amplification stage through the AD620 or instrumentation amplifier which is a differential amplifier that eliminates much of the noise. After this stage, the signal is filtered with a pass band, which has been designed to allow the passage of signals that are in the range of frequencies of the muscular movement of the sight, which is between 0 and 40 Hz. The implementation of low-pass and high-pass filters is carried out with a working frequency of 0.2 Hz and 40 Hz respectively, this creates a frequency window that allows reception and reading of

Fig. A3 EOG Electrode configuration of Dataset 2

the movements of the eye muscles. It is important to highlight that a conditioning circuit was implemented for vertical movement and another for horizontal movement. After conditioning, the signal goes to the ADC port of the FPGA card for its acquisition. For data reading, a sampling frequency of 120 Hz was used for approximately 2 seconds, which by Nyquist's sampling theory is always 2.5 times the maximum of the signal to be acquired in this case the movement of the sight it is between 0 and 40 Hz.

The EMG signals were recorded with a data acquisition equipment with a resolution of 10 bits, that is the reason why the data is in the range of 0 - 1024. 1024 being five volts of direct current. The EMG signals were recorded with a data acquisition equipment with a resolution of 10 bits, that is the reason why the data is in the range of 0 - 1024. 1024 being five volts of direct current. The activities carried out by each of the 10 subjects were: Up, Down, Right, Left, no movement (fixation in the center), and blinking.

2. Data Format

   The tasks of the subjects were separated by folders as detailed below:

- CN - Normal Behavior
- MD - Downward Movement
- ML - Movement to the left
- MP - Blink
- MR - Right movement
- MU - Upward Movement

Each folder contains 100 .CSV files, corresponding to the 10 tasks performed by each of the 10 subjects. These files were numbered randomly in each of the folders. Each file contains two columns corresponding to horizontal and vertical movement. In addition, each file contains 250 endpoints corresponding to a sampling of 120 data per second during the approximately 2 seconds of task completion.

Appendix B: MRMR Algorithm

The Minimum Redundancy Maximum Relevance (MRMR) Algorithm considers both feature relevancy with class label and feature redundancy among the selected features. Its formula is as follows:

$$J(x_k) = I(x_k; y) - \frac{1}{|S|} \sum_{x_j \in S} I(x_j; x_k) \tag{B1}$$

where $J(x_k)$ is the evaluation index, x_k is the candidate feature and S is the subset of the selected features. The MRMR algorithm is given below in Algorithm B1.

Algorithm B1: The MRMR Algorithm

Input: The traning dataset D with original feature set $F = \{f_1, f_2 \dots f_n\}$, class label Y and the required feature dimension T

Output: The selected subset feature S_T

$S_T \leftarrow \phi$
for f_i in F **do**
  $MI_i = I(f_i; y)$
  $f \leftarrow \max(MI)$;
  $S_T \cup f$;
  $F = F - f$
end for
for $i \leftarrow 2$ to T **do**
  for each f_i in F **do**
    $J(f_i) = MI_i - \frac{1}{|S|} \sum_{f_j \in S} I(f_k; f_i)$;
  end for
  select f_s from $J(f_i)$ with the largest value;
  $S_T = S_T \cup f_S$;
  $F = F - f_S$;
end for
return S_T

Appendix C: Parameters of SVM Models

Table C1: Parameters of Binary Classifier of EOG Signal Processor for Blink Detection

Parameters	**Binary Classifier**
W1	-7.5897
W2	-5.7514
W3	-12.7913
W4	-1.61449
Bias	7.3467
Kernel Function	Linear
Support Vectors	906 X 4 double

Table C2: Parameters of Multiclass Classifier of EOG Signal Processor for Multiclass Eye Movement Detection

Parameters	**Class 1**	**Class 2**	**Class 3**	**Class 4**	**Class 5**
W1	3.9123	6.4921	-4.2848	-2.9808	-1.7829
W2	5.4526	-5.8858	3.8359	1.0393	-2.1163
W3	-3.6949	-3.8014	1.8832	-1.9304	4.4051
W4	-4.4760	3.3457	-3.4405	7.0979	-2.7122
Bias	-6.899	-1.2857	-0.8653	-0.2961	2.0947
Kernel Function	Linear	Linear	Linear	Linear	Linear
Support Vectors	130 X 4 double	154 X 4 double	162 X 4 double	163 X 4 double	119 X 4 double

Appendix D: Overview of the selected modules

ZedBoard™ is a low-cost development board for the Xilinx Zynq®-7000 SoC. This board contains everything necessary to create a Linux, Android, Windows® or other OS/RTOS-based design. Additionally, several expansion connectors expose the processing system and programmable logic I/Os for easy user access. Take advantage of the Zynq-7000 SoC's tightly coupled ARM® processing system and 7 series programmable logic to create unique and powerful designs with the ZedBoard.

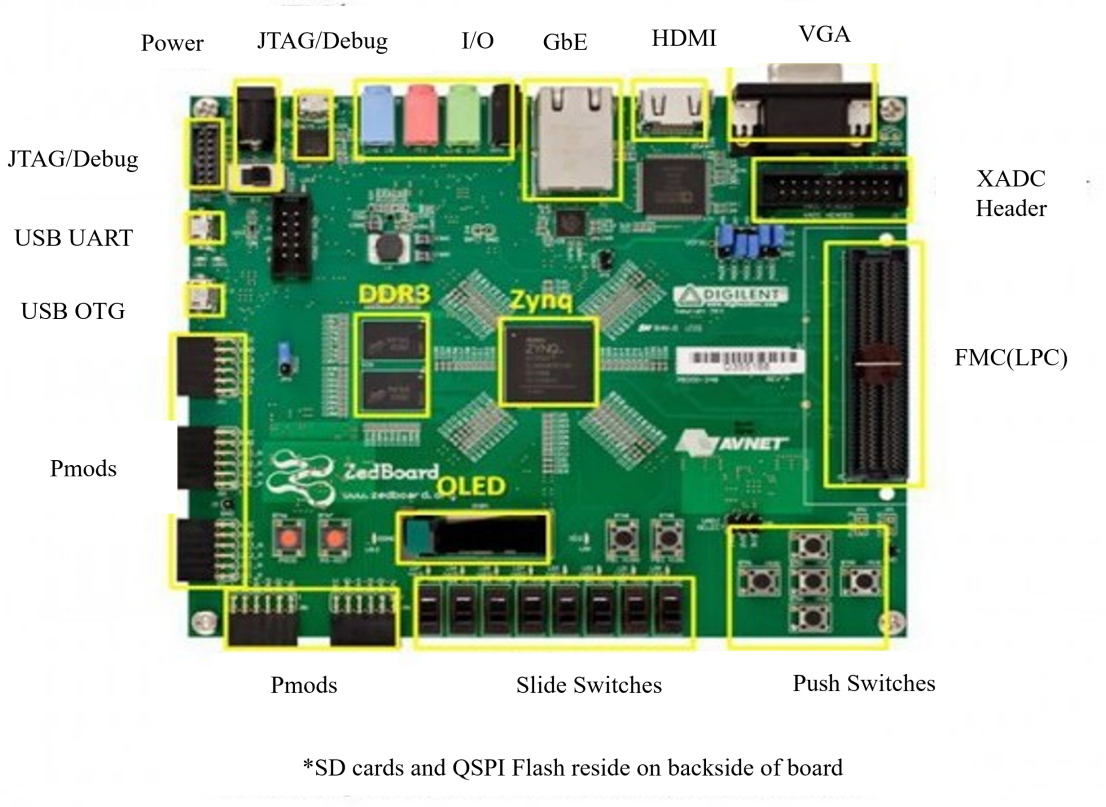


Fig. D4 Overview of ZedBoard Zynq Evaluation and Development Kit

Key Features and Benefits

- Zynq-7000 SoC XC7Z020-CLG484-1
- 512 MB DDR3
- 256 Mb Quad-SPI Flash
- 4 GB SD card
- Onboard USB-JTAG Programming
- 10/100/1000 Ethernet
- USB OTG 2.0 and USB-UART
- PS & PL I/O expansion (FMC, Pmod™, XADC)
- Multiple displays (1080p HDMI, 8-bit VGA, 128 x 32 OLED)
- I2S Audio CODEC

What's Included

- 12 V AC/DC power supply
- Avnet ZedBoard 7020 baseboard
- Getting Started Guide
- Micro-USB cable
- USB Adapter: Male Micro-B to Female Standard-A
- Xilinx Vivado® Design Edition license voucher (device locked to 7Z020)

Fig. D5 Specifications of ZedBoard

The ZCU106 Evaluation Kit enables designers to jumpstart designs for video conferencing, surveillance, Advanced Driver Assisted Systems (ADAS) and streaming and encoding applications. This kit features a Zynq™ UltraScale+™ MPSoC EV device and supports all major peripherals and interfaces, enabling development for a wide range of applications. The included ZU7EV device is equipped with a quad-core Arm® Cortex®-A53 applications processor, dual-core Cortex-R5 real-time processor, Mali™-400 MP2 graphics processing unit, 4KP60 capable H.264/H.265 video codec, and 16nm FinFET+ programmable logic.

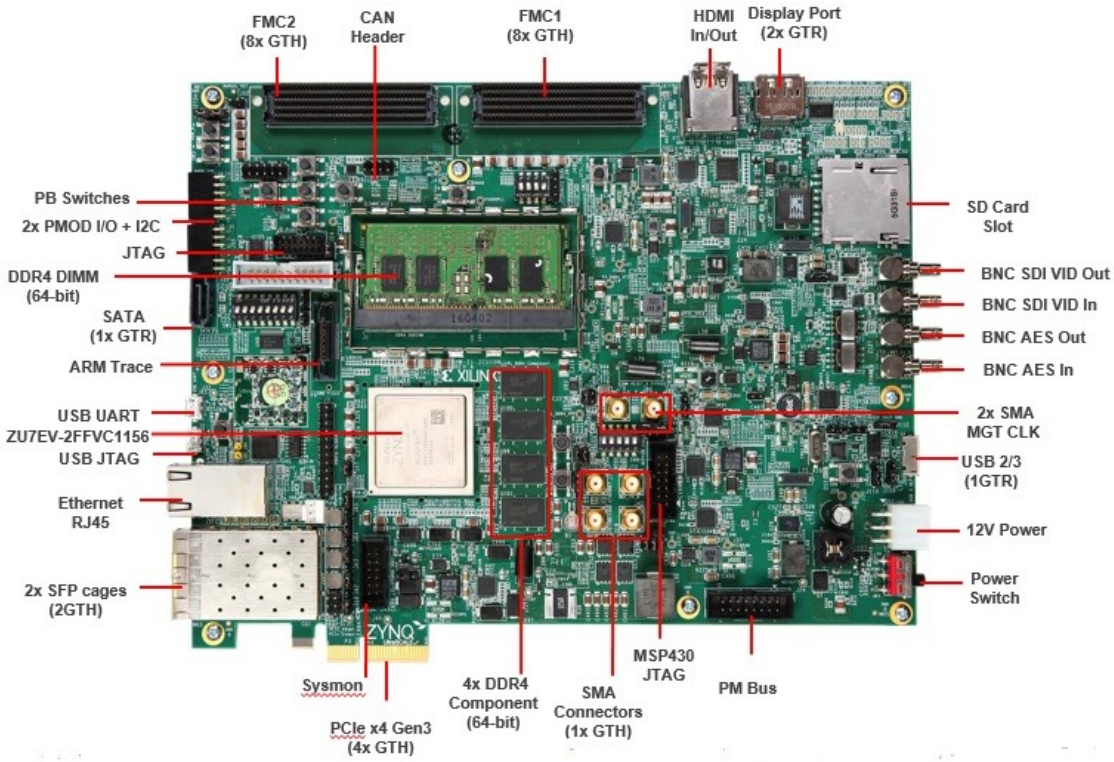


Fig. D6 Overview of Zynq Ultrascale+ ZCU106 Evaluation Platform

Configuration

- Onboard JTAG circuitry to enable configuration over USB
- Dual quad-SPI flash memory
- Boot from SD card

Memory

- PS DDR4 72-bit SODIMM
- PL DDR4 component
- Quad-SPI flash
- SD card slot

Control & I/O

- 6x directional pushbuttons
- DIP switches
- PMBUS & System Controller MSP430 for power, clocks, and I2C bus switching
- USB2/3

Expansion Connectors

- 2x FMC-HPC connectors
- 2 Pmod headers

Communication & Networking

- SDI (x1 GTH)
- AES3 audio connector
- SFP+ cage (2x 2GTH)
- SMA (x1 GTH)
- UART to USB bridge
- RJ-45 Ethernet connector
- SATA (1x GTR)
- PCIe Gen3 Endpoint (x4 GTH)

Display

- HDMI video input and output (x3 GTH)
- DisplayPort (2x GTR)

Clocking

- Programmable clocks
- System clocks, user clocks, jitter attenuated clocks

Power

- 12V wall adaptor or ATX

Fig. D7 Specifications of Zynq UltraScale+ XCZU7EV-2FFVC1156 MPSoC

Appendix E: Design in Xilinx System Generator

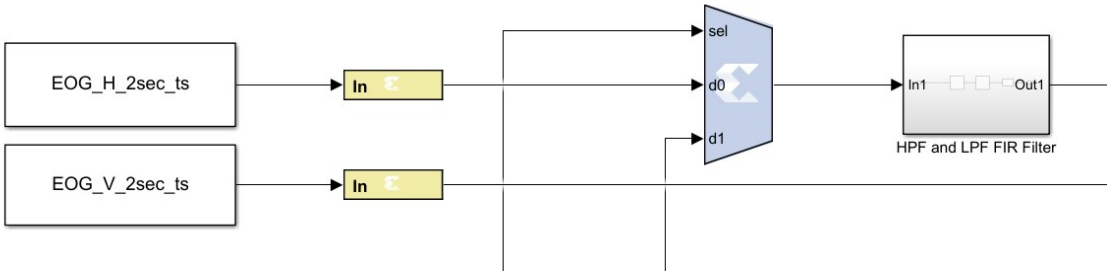


Fig. E1 Dual channel EOG data is taken in parallel

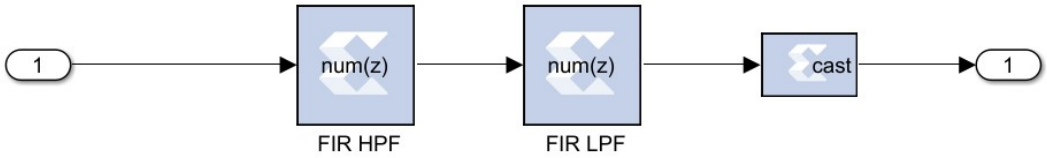


Fig. E2 Filter Unit of EOG Signal Processor

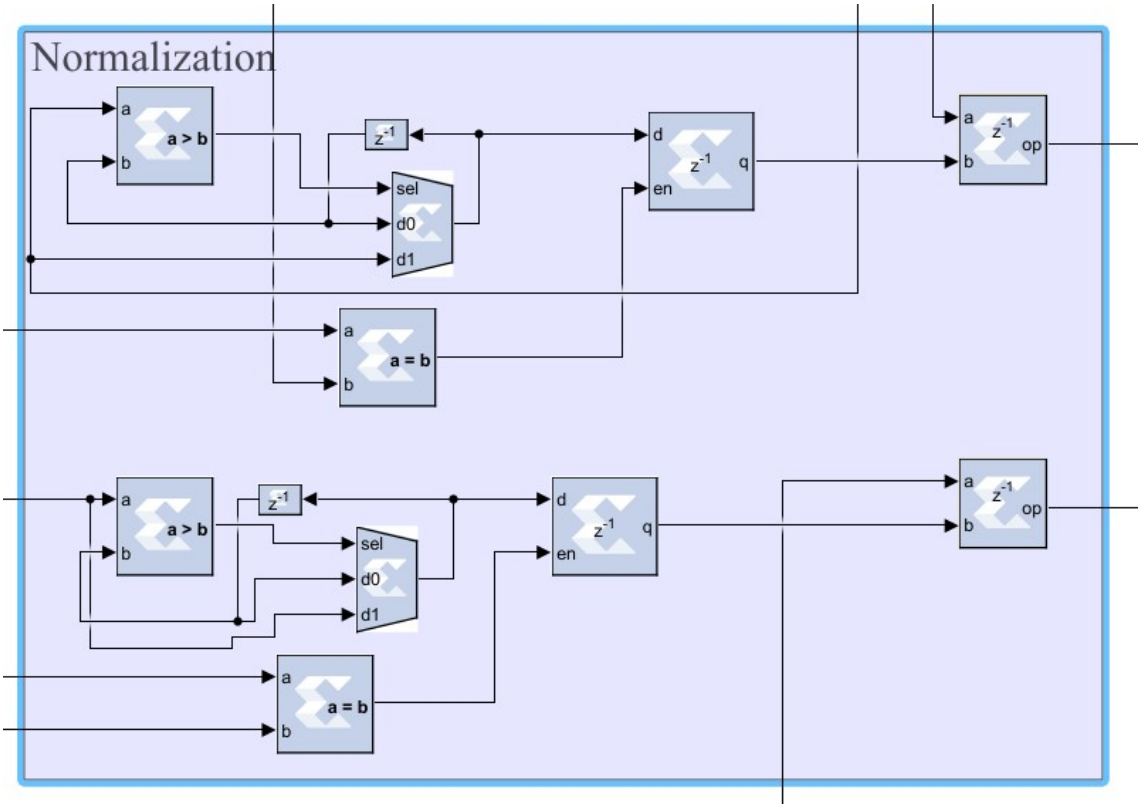


Fig. E3 Normalization Unit of EOG Signal Processor

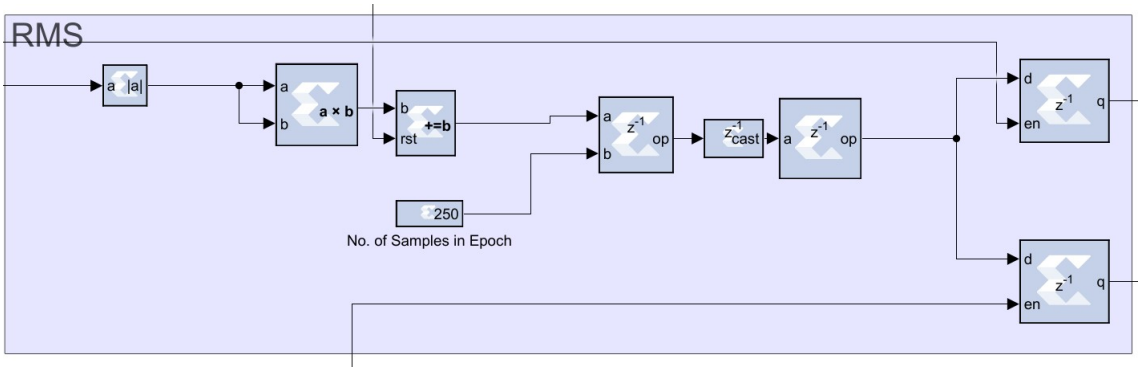


Fig. E4 RMS Extractor of EOG Signal Processor

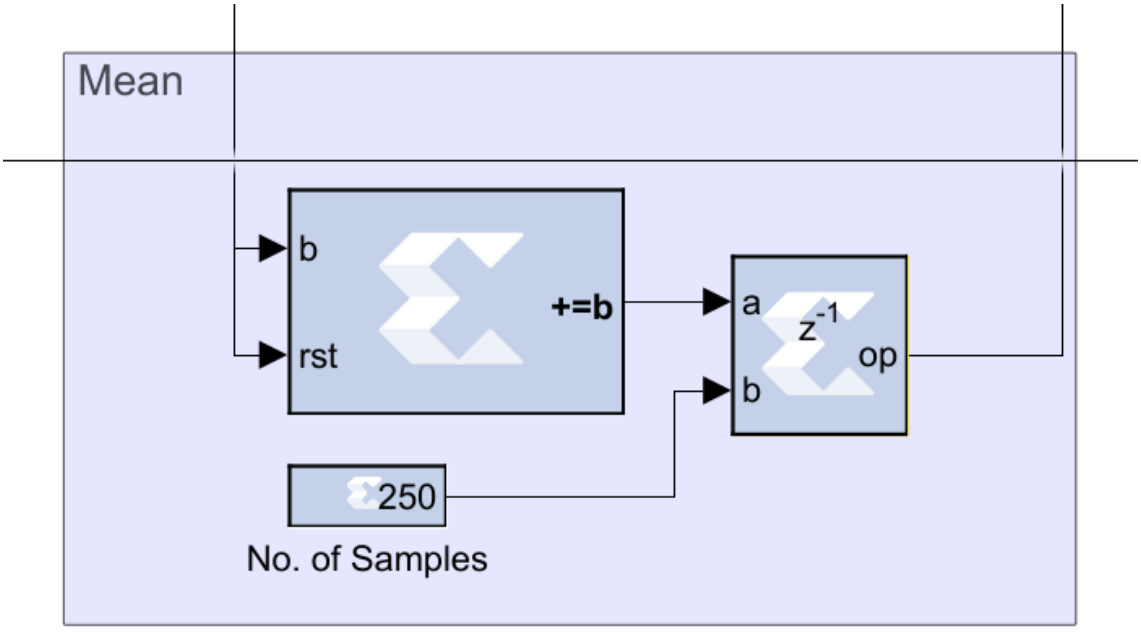


Fig. E5 Mean Extractor of EOG Signal Processor

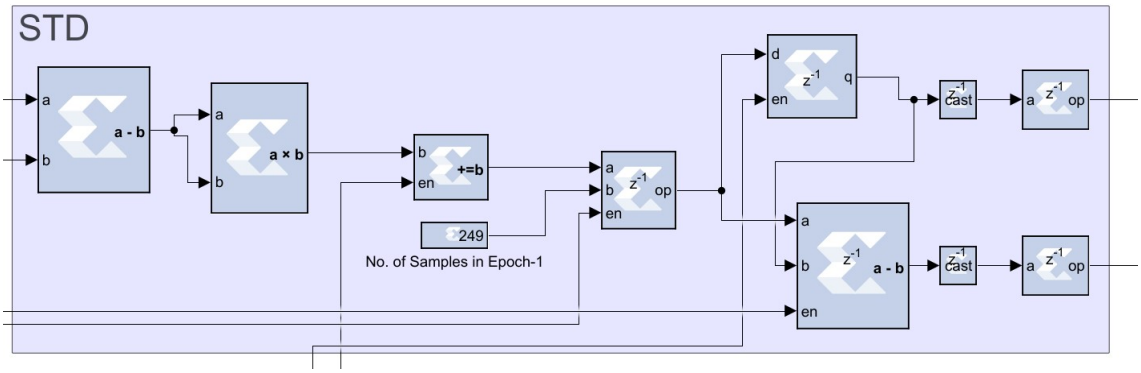


Fig. E6 STD Extractor of EOG Signal Processor

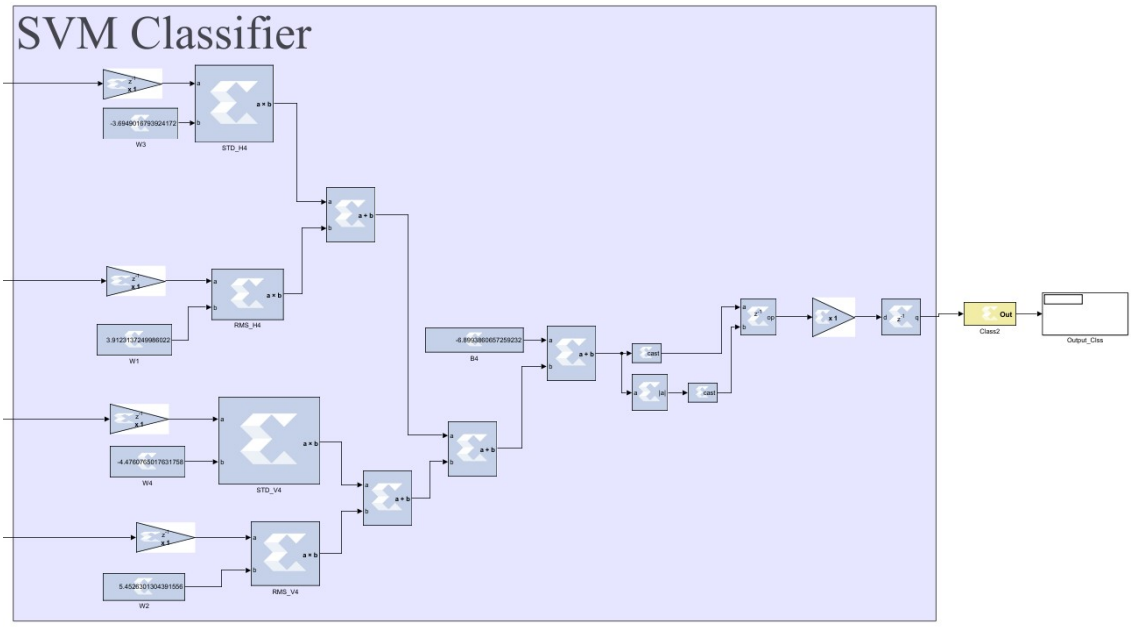


Fig. E7 Binary SVM classifier of EOG Signal Processor

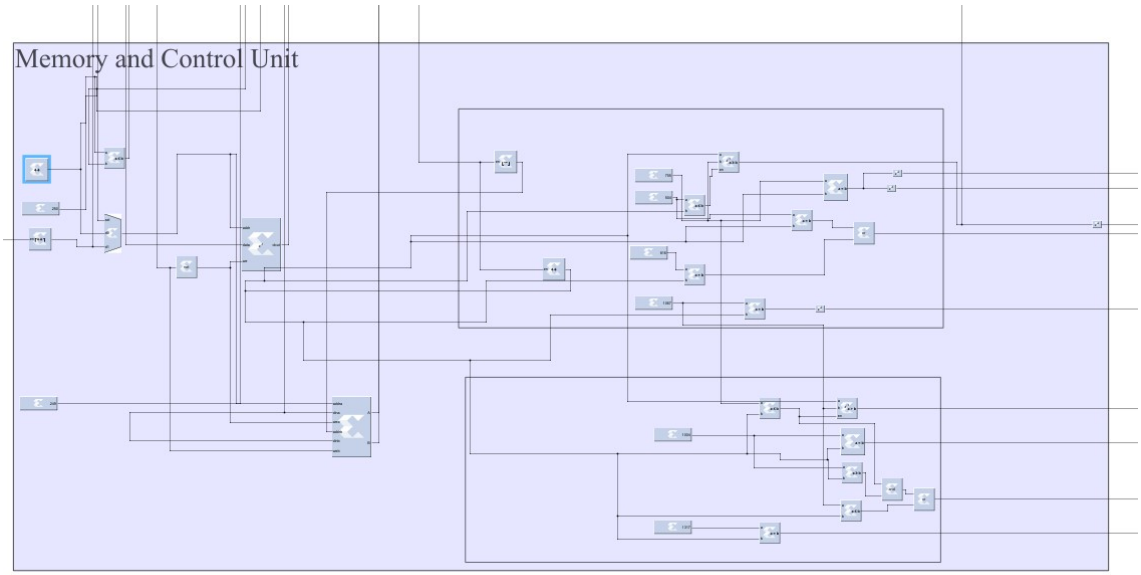


Fig. E8 Control and Memory Unit of EOG Signal Processor

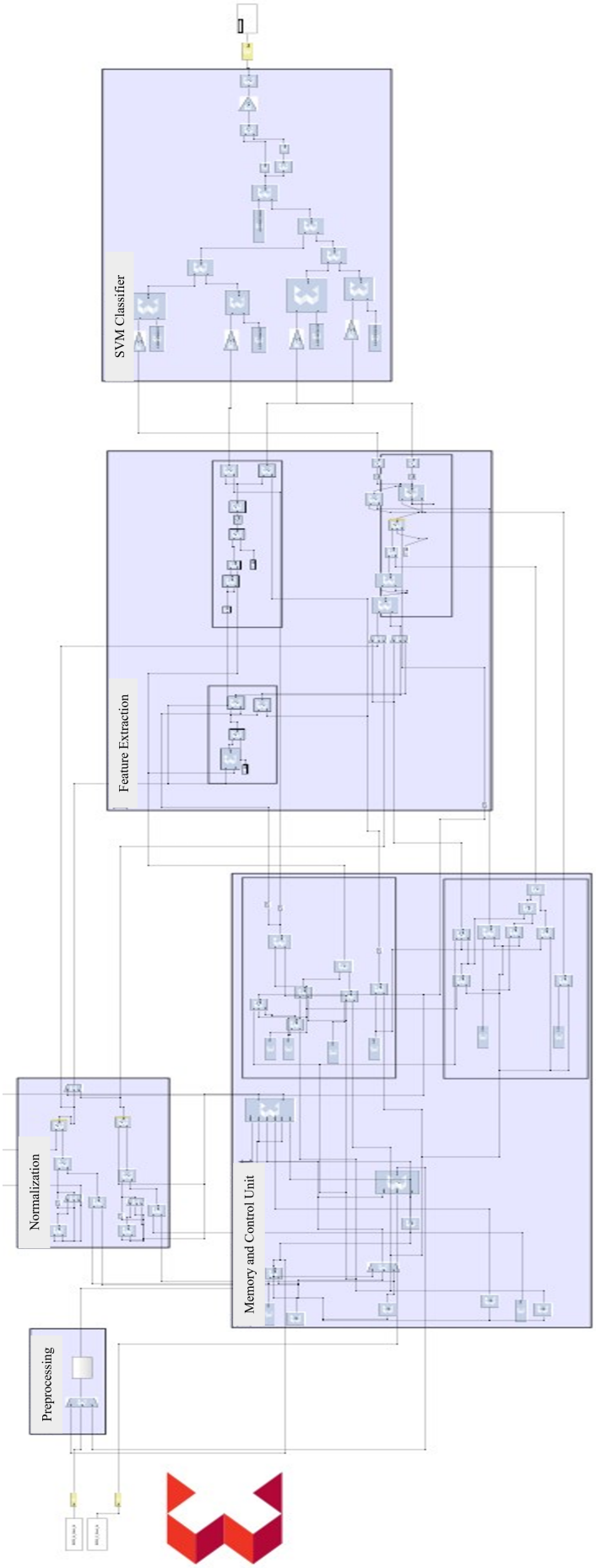


Fig. E9 Compact EOG Signal Processor for Binary Classification

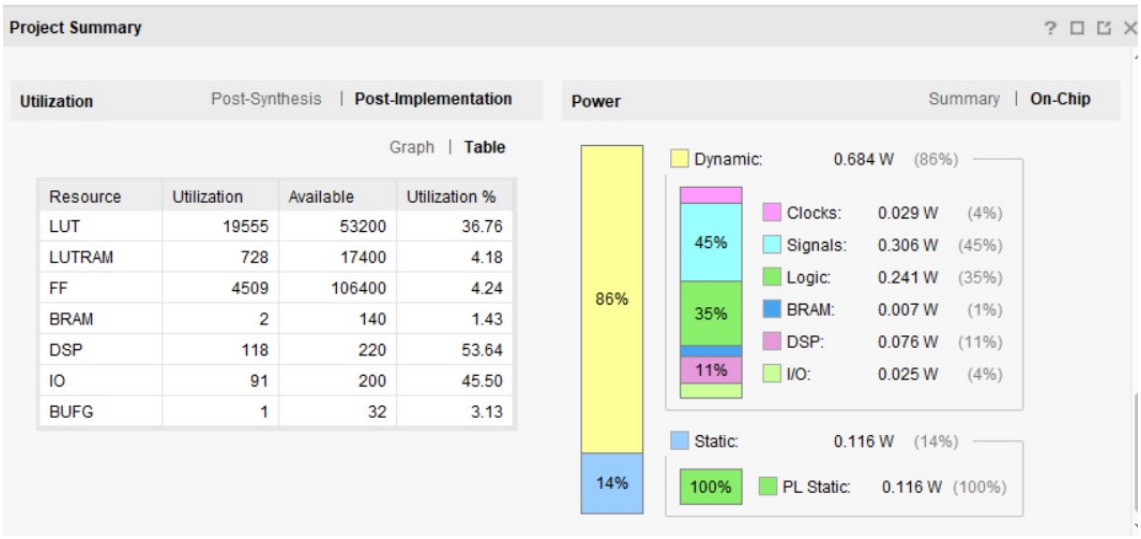


Fig. E10 Summary of implemented Binary EOG signal processor in ZedBoard

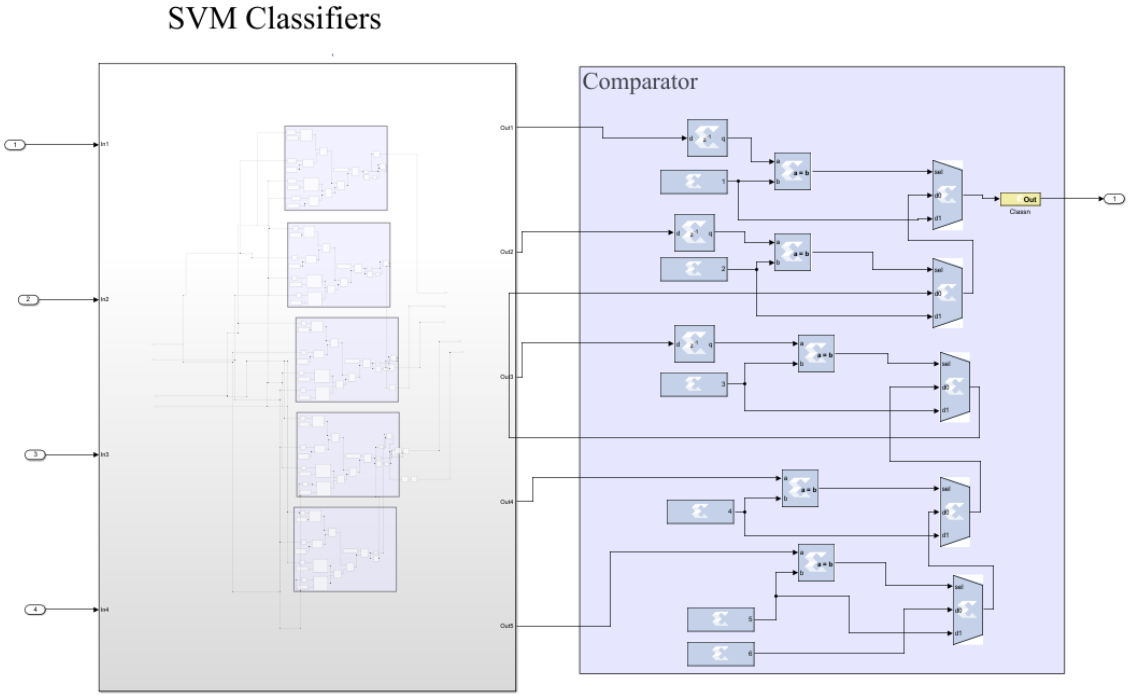


Fig. E11 Multiclass Classifier with Comparing Logic

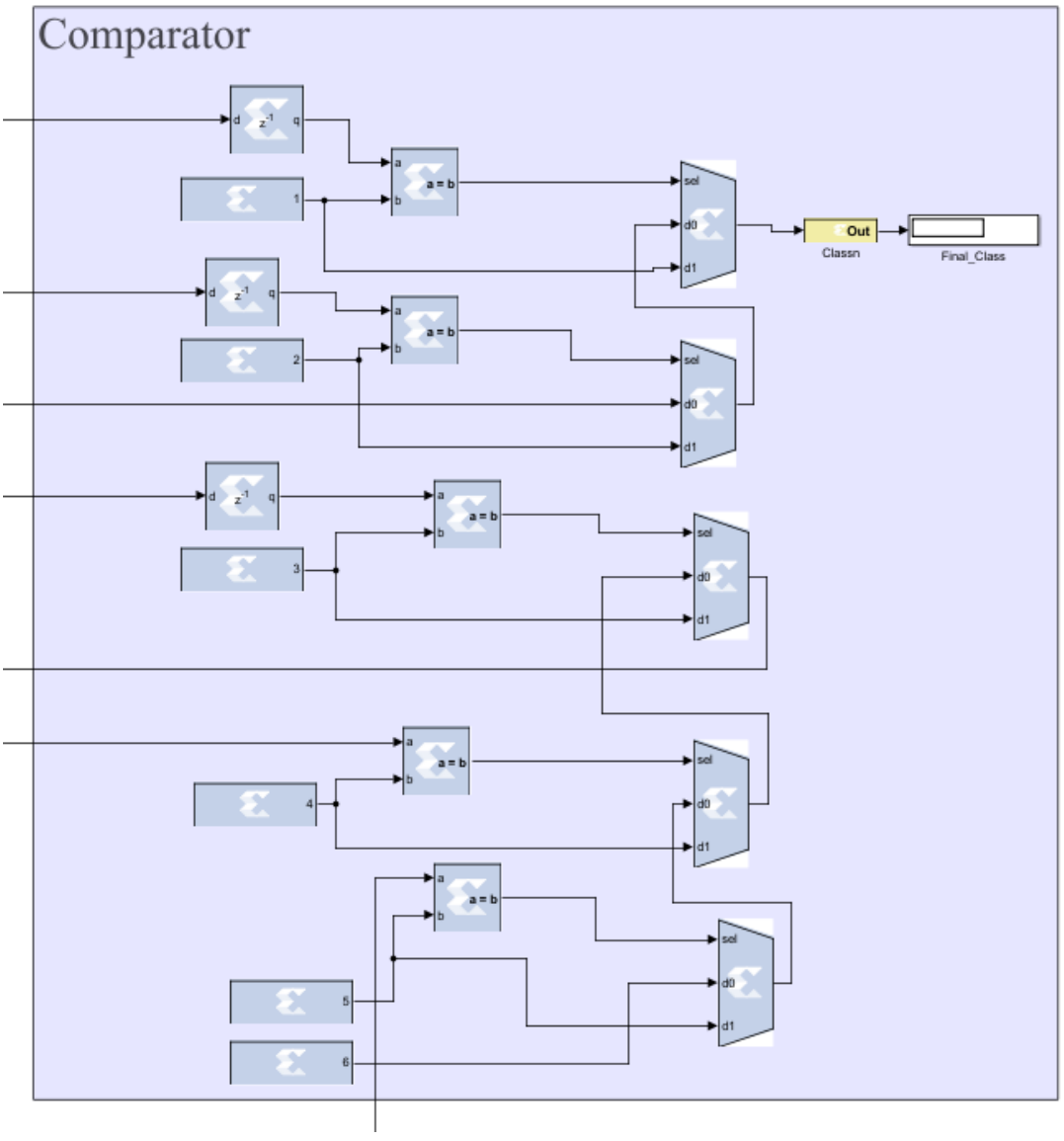


Fig. E12 Comparator used in Multiclass Classifier of EOG Processor

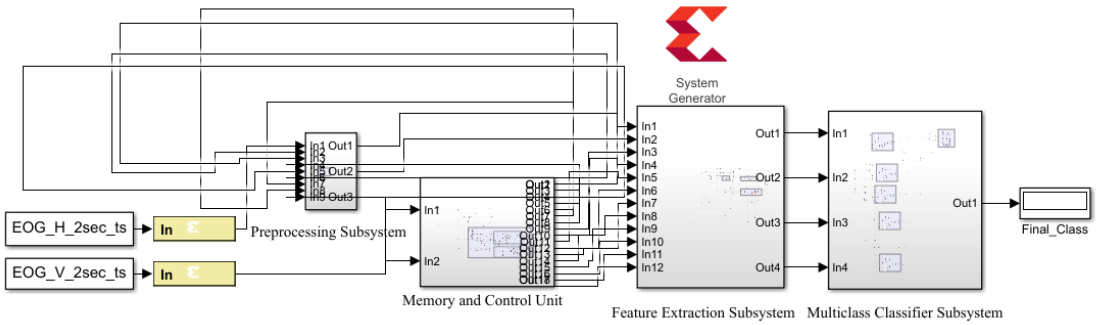


Fig. E13 Compact EOG Signal Processor for Multiclass Classification

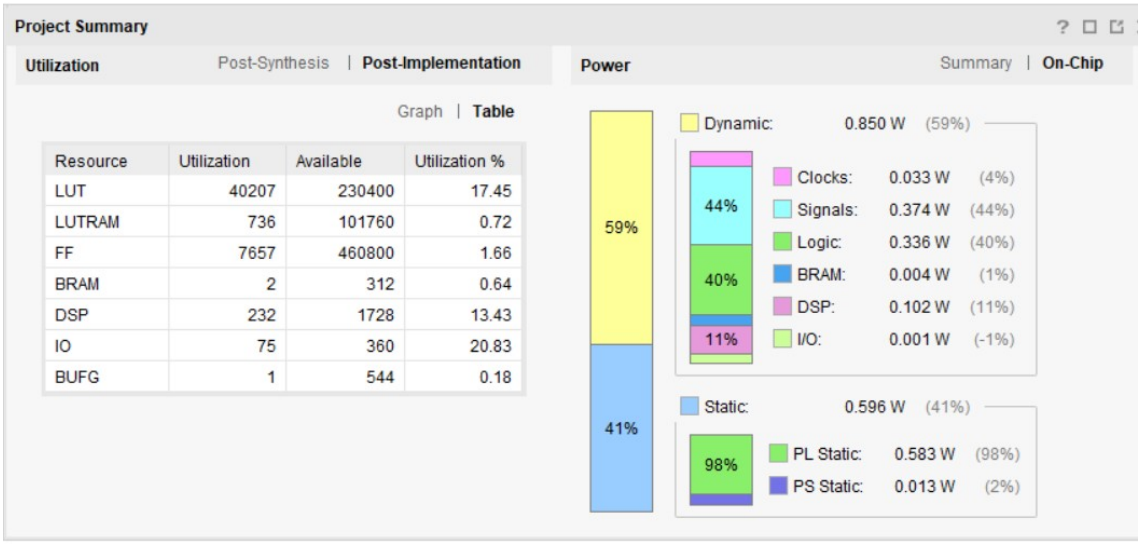
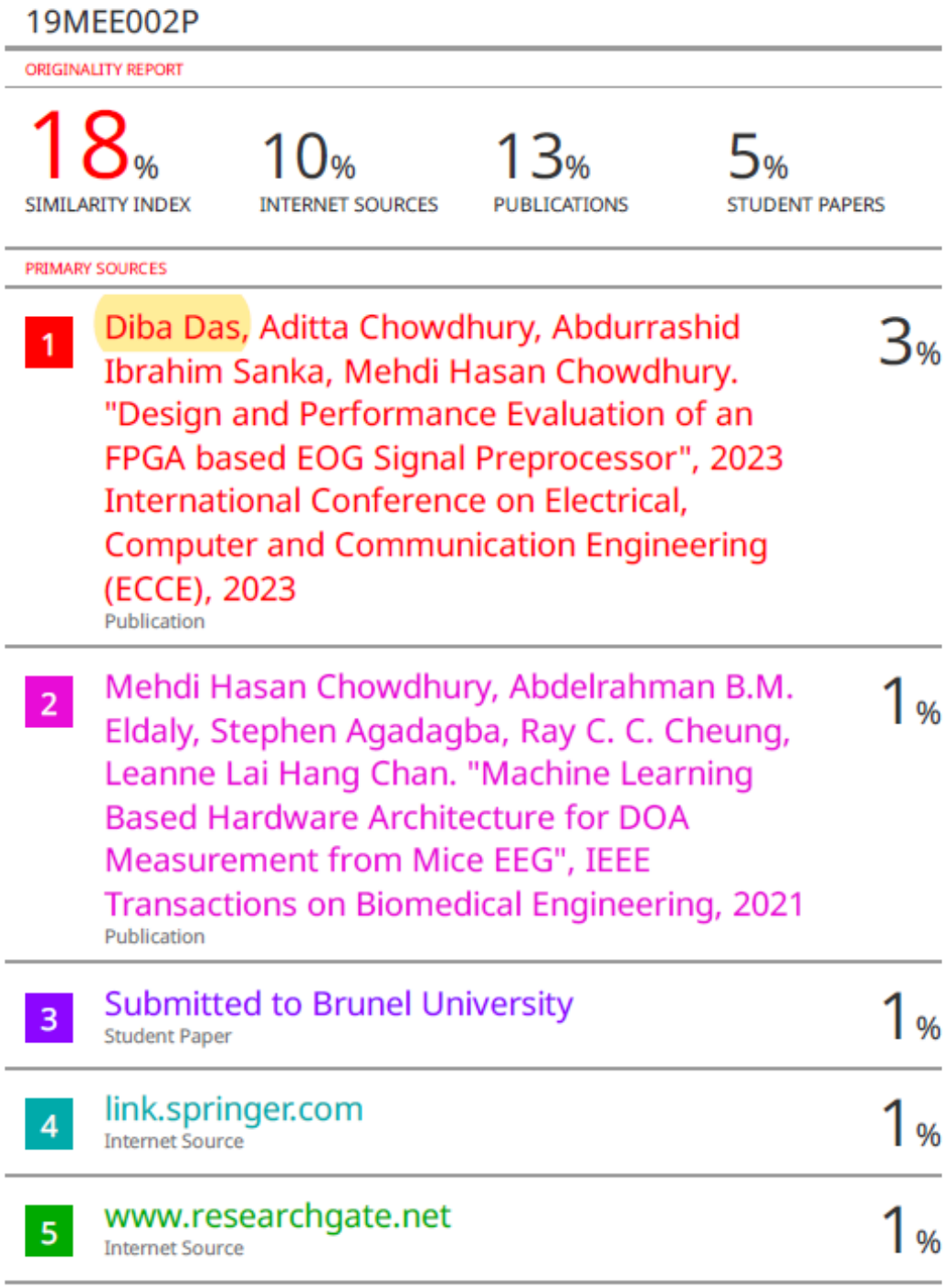


Fig. E14 Summary of implemented Multiclass EOG signal processor in Zynq Ultrascale+

Appendix E: Similarity Index Report



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ORIGINALITY REPORT

18%	10%	13%	5%
SIMILARITY INDEX	INTERNET SOURCES	PUBLICATIONS	STUDENT PAPERS

PRIMARY SOURCES

1	Diba Das, Aditta Chowdhury, Abdurrashid Ibrahim Sanka, Mehdi Hasan Chowdhury. "Design and Performance Evaluation of an FPGA based EOG Signal Preprocessor", 2023 International Conference on Electrical, Computer and Communication Engineering (ECCE), 2023 Publication	3%
2	Mehdi Hasan Chowdhury, Abdelrahman B.M. Eldaly, Stephen Agadagba, Ray C. C. Cheung, Leanne Lai Hang Chan. "Machine Learning Based Hardware Architecture for DOA Measurement from Mice EEG", IEEE Transactions on Biomedical Engineering, 2021 Publication	1%
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